SC7000/B1

(RM03/RM05/RM80 COMPATIBLE)

DISK CONTROLLER

TECHNICAL MANUAL

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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EMULEX PRODUCT WARRANTY

DISK CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex disk controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

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Section 1
GENERAL DESCRIPTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC7000 Disk Controller manufactured by Emulex Corporation. This manual also provides diagnostic and application information.

The contents of the eight sections and four appendices in this manual are briefly outlined in the following descriptions:

Section 1 **General Description:** This section contains an overview of the SC7000 Disk Controller and describes features, compatibility, and performance.

Section 2 **Specifications:** This section presents electrical and physical specifications for the SC7000 Disk Controller and V-MASTER in tabular form for easy reference.

Section 3 **Applications and Configurations:** This section describes configuration of applications to help the user choose bus addresses, interrupt vector addresses, and mapping of logical/physical disk drives for optimum system performance.

Section 4 **Installation:** This section contains the information necessary to set-up and physically install the SC7000 Disk Controller system.

Section 5 **Troubleshooting:** This section describes fault isolation procedures that can be used to pinpoint trouble spots.

Section 6 **Registers, Commands and Programming:** This section contains descriptions of all MBA and device registers in the Controller, and of commands and programming techniques which are used to operate the Controller.

Section 7 **Functional Description:** This section contains a description of controller architecture and formats used on the disk drives to help the programmer write effective programs.

Section 8 **Interfaces:** This section contains pin/signal assignments for the CPU and peripheral interfaces.

Appendix A **SC7000/Bl Configuration and Option Selection:** This appendix lists the disk drives and configurations supported by the SC7000 Disk Controller firmware.

Appendix B **Disk Drive Modifications:** This appendix describes modifications that can be made to move Index and Sector signals from the A-Cable to the B-Cable on commonly used disk drives.

Appendix C **Diagnostic Operations:** This appendix contains the procedure for running the DEC RH750 and RH780 and RM03/RM05/RM80 diagnostic programs.

Appendix D **VAX Numbers Quick Reference:** This appendix lists and defines Base Addresses and byte offsets used in VAX CPU systems.

This section is divided into five subsections, as listed in the following table:

Subsection	Title
1.1	Scope
1.2	Overview
1.3	Physical Description
1.4	Features
1.5	Functional Compatibility

1.2 OVERVIEW

The SC7000 Disk Controller is a single extended hex-sized printed circuit board assembly (PCBA) which can be plugged directly into slot seven, eight, or nine of a Digital Equipment Corporation (DEC) VAX-11/750 central processing unit (CPU) backplane or expansion box, or which can become a component of an Emulex V-MASTER/780 unit.

When embedded as a single PCBA in the VAX-11/750 CPU, the SC7000 Disk Controller provides a CPU Memory Interface (CMI) and a complete functional emulation of a Digital Equipment Corporation (DEC) RH750 Massbus Adapter (MBA) and up to eight logical RM03, RM05 or RM80 disk drives which can be mapped on up to four physical disk drives that have Storage Module Drive (SMD) interface.

When used with the Emulex V-MASTER/780 card cage assembly, the SC7000 Disk Controller provides a V-MASTER Interface (VMI) and a complete functional emulation of a DEC RH780 MBA and up to eight logical RM03, RM05 or RM80 disk drives which can be mapped on up to four physical disk drives that have SMD interface.

The SC7000 Disk Controller includes an associated Cable Paddleboard PCBA that provides Storage Module Drive (SMD) interface with up to four physical disk drives.

1.3 PHYSICAL DESCRIPTION

The SC7000 Disk Controller PCBA [part number (P/N) SU7510410], the Cable Paddleboard PCBA (P/N SU7810404), the Bus Interface PCBA (P/N SU7810401), and the Bus Translator PCBA (P/N SU7810402 revision D or later, or P/N SU7810409) are shown in Figure 1-1. In the VAX-11/750 CPU system, only the SC7000 Disk Controller PCBA and the Cable Paddleboard PCBA (P/N SU7510402) are required.

1.3.1 DISK CONTROLLER

The SC7000 Disk Controller consists of a single PCBA which plugs into one of the two controller slots in the V-MASTER/780 card cage, or into slot seven, eight, or nine in the VAX-11/750 CPU backplane. A Cable Paddleboard PCBA plugs onto the pins at the rear of the backplane connector that is used for the SC7000 Disk Controller PCBA. The Cable Paddleboard PCBA provides connection for the disk drive A-Cable and up to four B-Cables. The A-Cable can be daisy chained, but the B-Cables are radially connected, one to each disk drive.

1.3.2 V-MASTER/780 ASSEMBLY

The V-MASTER/780 assembly is a unique new approach for interfacing mass-storage peripherals to the DEC VAX-11/780 CPU. It consists of a four-slot, wire-frame, card cage with an integral backplane and two Synchronous Backplane Interface (SBI) PCBAs; the Bus Interface PCBA and Bus Translator PCBA in slots one and two, respectively. Slots three and four can each accommodate one SC7000, SC780, or SC788 Disk Controller PCBA, or one TC7000 Tape Coupler PCBA (one Cable Paddleboard PCBA is required for each SC7000 Disk Controller PCBA). The card cage is designed to mount in the DEC VAX-11/780 CPU cabinet in place of the DEC RH780 MBA or the SBI terminator. This architecture allows Emulex to install two SC7000 Disk Controllers in the same space that a single DEC RH780 MBA occupies.

1.4 FEATURES

The SC7000 Disk Controller design incorporates several features that enhance usefulness, serviceability, and performance. Emulex disk controllers achieve performance that exceeds the performance of DEC controllers, which they emulate, by providing enhancement features such as built-in self test during power-up, and built-in optional selection of storage capacities, etc. which are not available on the DEC RH750 or RH780 MBAs.

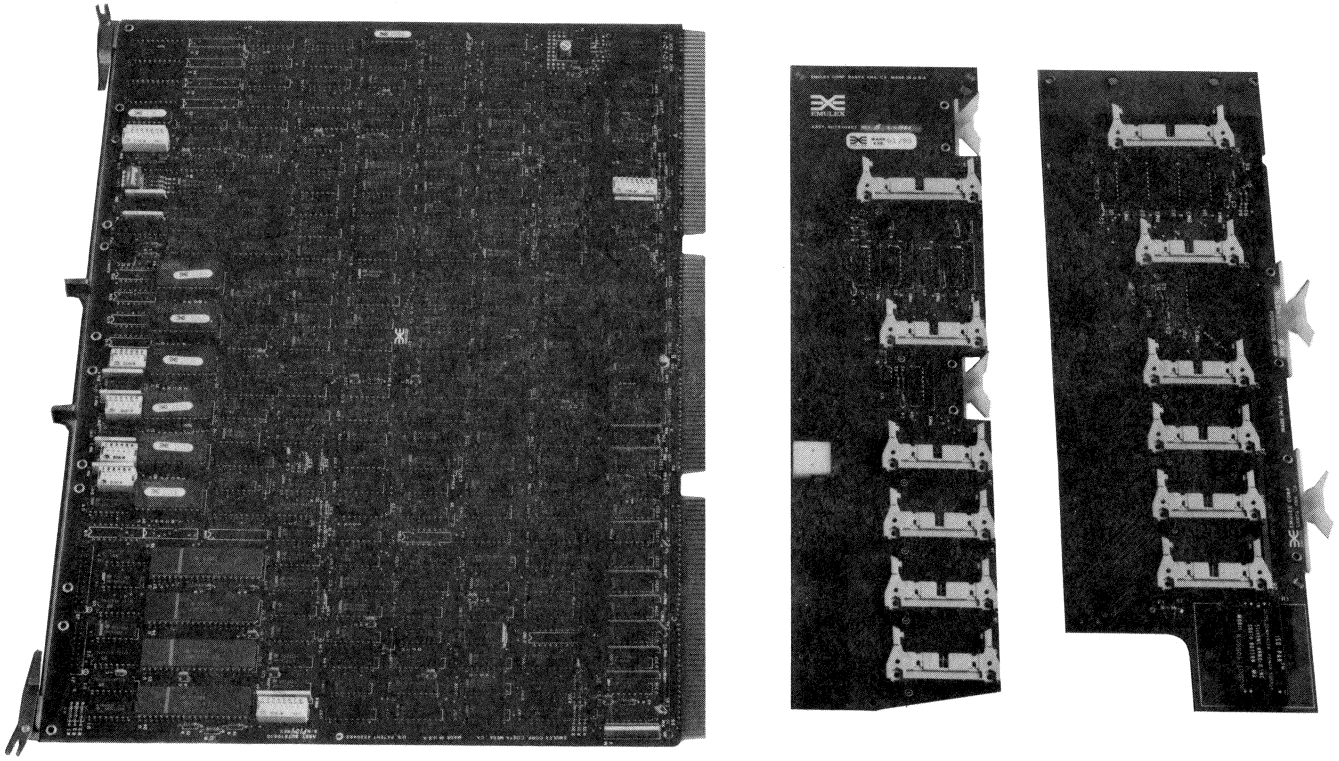

Figure 1-1. SC7000 PCBA and Cable Paddleboards

1.4.1 MICROPROCESSOR DESIGN

The SC7000 Disk Controller design incorporates a unique 16-bit, high-speed, bipolar microprocessor that performs all the controller functions. The microprocessor design approach provides a reduced component count, high reliability, easy maintainability, and the means to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The microprocessor is constructed from AMD 2901 bit-slice components and executes microinstructions in 125 nanoseconds. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various capacities.

1.4.2 PACKAGING

The SC7000 Disk Controller is constructed as a single, extended, hex-sized multiple-layer PCBA, and plugs into the VAX-11/750 CPU back plane or into the V-MASTER/780 card cage. Each SC7000 Disk Controller is associated with a Cable Paddleboard PCBA that plugs onto the back of the same backplane connector as used by the controller, but at the back of the card cage backplane.

1.4.3 SELF-TEST

The SC7000 Disk Controller incorporates an internal Self-Test routine which is executed when the computer system is powered up. This test exercises all parts of the microprocessor, buffer, and data-handling logic. Successful completion of the Self Test indicates high probability that all circuits in the SC7000 Disk Controller are operational. If the SC7000 Disk Controller fails the Self-Test operation, the FAULT LED on the front edge of the SC7000 Disk Controller PCBA illuminates and the SC7000 Disk Controller cannot be addressed from the CPU.

1.4.4 BUFFERING

The SC7000 Disk Controller contains a 4K x 16-bit high-speed RAM which stores the contents of the MBA registers of the controller, and the disk drive (device) registers for up to eight logical disk drive units, and provides 12 sectors of data buffering.

1.4.5 ERROR CORRECTION

The SC7000 Disk Controller incorporates a 32-bit error correcting code (ECC) which can correct single error bursts of up to 11 bits long and detect error bursts of longer length. The SC7000 Disk Controller determines the location of the error and the error pattern and then passes this information back to the CPU which actually performs the correction of the erroneous data. A 16-bit CRCC is used with the header of every sector.

1.4.6 OPTION AND CONFIGURATION SWITCHES

Two eight-pole DIP switches, four six-pole DIP switches, and two four-pole DIP switches are used to configure the SC7000 Disk Controller for various disk drive capacities (sizes), certain firmware options, MBA number and arbitration level. It is possible to select any one of 64 possible disk drive configurations for each of the four physical disk drives which can be handled by the SC7000 Disk Controller, including mixtures of disk capacities and disk drive type codes.

1.4.7 GET CHARACTERISTICS CAPABILITY

Since the SC7000 Disk Controller can handle a number of different disk drive sizes, a capability has been provided to read out the maximum cylinder, maximum track, and maximum sector address, as well as the selected disk drive type code. This capability allows self-configuring software to handle different disk drive configurations and capacities on the same controller.

1.4.8 DUAL-PORT CAPABILITY

The SC7000 Disk Controller can operate with disk drives that have dual-port capability. This feature allows a second SC7000 Disk Controller to have access to the disk drives on a priority (time-sharing) basis.

1.5 FUNCTIONAL COMPATIBILITY

The SC7000 Disk Controller is compatible with functionality, media, diagnostics, and operating systems to the extent described in this subsection.

1.5.1 FUNCTIONALITY

The SC7000 Disk Controller is functionally compatible with the DEC RH750 and RH780 MBAs with one or more RM-type disk drives attached, except the SC7000 Disk Controller does not execute the Diagnostic mode of the RH750 or RH780 MBAs or the Maintenance mode of the RM80 disk drive. The absence of the Diagnostic mode prevents running the complete RH750 and RH780 Diagnostic programs.

1.5.2 MEDIA COMPATIBILITY

The SC7000 Disk Controller is media compatible with the DEC RM02/RM03 disk packs when using a Control Data Corporation (CDC) 9762 disk drive or equivalent, and with the DEC RM05 disk pack when using a CDC 9766 disk drive or equivalent. There is no need for media compatibility with the RM80 disk pack because it is a fixed-media disk drive, but the format is the same as used by the DEC RM80 disk drive.

1.5.3 DIAGNOSTICS

The SC7000 Disk Controller, when configured for an unexpanded-size disk drive, is compatible with the following standard DEC RM03, RM05 and RM80 diagnostic programs:

EVRAA	VAX RP/RK/RM/RX/TU58 Reliability
EVRAC	Disk Formatter
EVRDB	RM03/RM05 Functional Diagnostic
EVRGA	RM80 Formatter
EVRGB	RM80 Functional Diagnostic

Emulex also provides, in a separate manual, supporting diagnostic programs for the SC7000 Disk Controller (order Emulex manual P/N VX9951002).

1.5.4 OPERATING SYSTEMS

When emulating standard capacity (size) RM03, RM05 or RM80 disk drives, the SC7000 Disk Controller is compatible with the VAX/VMS operating system. Nonstandard sized disk drives can be used by appropriate patching to the disk drive and bootstrapping facility.

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2.1 OVERVIEW

This section contains the general, electrical, and physical specifications for the SC7000 Disk Controller. This section is divided into four subsections, as listed in the following table:

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications
2.4	V-MASTER Specifications

2.2 GENERAL AND ELECTRICAL SPECIFICATIONS

General and electrical specifications for the SC7000 Disk Controller are listed and described in Table 2-1.

Table 2-1. SC7000 Disk Controller General and Electrical Specifications

Parameter	Description
GENERAL FUNCTIONS	
Emulation	DEC RM03, RM05 and RM80 disk drives DEC RH750 and RH780 MBAs
Media Compatibility	DEC RM03 and RM05 when using appropriate disk drives
Disk Drive Interface	SMD
Disk Drive Ports	4
Error Control	32-bit ECC for data and 16-bit CRCC for headers. Correction of single data error burst up to 11 bits long.
Sector Capacity:	512 bytes

Table 2-1. SC7000 Disk Controller General and Electrical Specifications (continued)

Parameter	Description
GENERAL FUNCTIONS (cont'd)	
Sectors/Track	Selectable for each disk drive
Tracks/Cylinder	Selectable for each disk drive
Cylinders/Disk Drive	Selectable for each disk drive
Disk Drive Type Code	Selectable for each disk drive
Computer Interface	VAX-11/750: CMI V-MASTER/780: SBI VAX-11/780: VMI
Nexus Address	VAX-11/750: RH0, RH1, RH2 VAX-11/780: TR4 -- TR11
Interrupt Priority	BR5 for VAX-11/750 BR4 -- BR7 for VAX-11/780 (selection is made externally to SC7000 Disk Controller PCBA)
Data Buffering	12 full sectors
Data Transfer	32-bit DMA via CMI 64-bit DMA via SBI
Self Test	Extensive internal Self-Test routine on power-up
Design	High-speed bipolar microprocessor with AMD 2901 bit-slice components
ELECTRICAL	
SBI Interface	DEC approved line drivers and receivers
CMI Interface	DEC approved line drivers and receivers
Disk Drive Interface	Differential line drivers and receivers. A-Cable accumulative length to 100 feet. B-Cable length to 50 feet.
Power Required	+5 Volts Direct Current (Vdc), 10 Amperes (A) with one 4-port SC7000 Disk Controller in a V-MASTER/780 -15 Vdc, 1 A maximum (VAX-11/750)

2.3 PHYSICAL SPECIFICATIONS

Physical specifications for the SC7000 Disk Controller are listed and described in Table 2-2.

Table 2-2. SC7000 Disk Controller Physical Specifications

Parameter	Description
PHYSICAL	
Packaging	SC7000 Disk Controller PCBA - One DEC extended hex-sized PCBA Cable Paddleboard PCBA
Mounting	Massbus controller slot 7, 8 or 9 in VAX-11/750 CPU backplane V-MASTER/780 chassis
Disk Drive Connections	Cable Paddleboard PCBA on rear of backplane has connectors for A-Cable and B-Cables
OPERATING ENVIRONMENT	
Temperature	50 to 104° Fahrenheit (°F) - or - 10 to 40 ° Celsius (°C)
Temperature Gradient	18° F (10° C) per hour, maximum
Relative Humidity	20 to 80 %, noncondensing
NONOPERATING ENVIRONMENT	
Temperature	-40° to +150° F (-40° to 65.5° C)
Relative Humidity	5 to 95 %, noncondensing

2.4 V-MASTER SPECIFICATIONS

Specifications for the V-MASTER/780 are listed and described in Table 2-3.

Table 2-3. V-MASTER/780 Specifications

Parameter	Description
CARD CAGE	
Type	Wire frame
Slots	4 Slot #1 for Bus Interface PCBA Slot #2 for Bus Translator PCBA Slot #3 for first SC7000 PCBA Slot #4 for second SC7000 PCBA
PCBAs	Bus Interface PCBA (P/N SU7810401) Bus Translator PCBA (P/N SU7810402 Rev D or later, or P/N SU7810409)
Backplane	SBI
Replaces	DEC RH780 MBA or SBI Terminator Module in VAX-11/780 CPU backplane
Power Required	DEC or Emulex power supply: -5.2 Vdc, 1 A maximum (VAX-11/780) +5.0 Vdc, 34 A maximum from DEC or Emulex power supply when two controllers are installed in V-MASTER/780
Dimensions	3.125 inches (in.) Wide 20 in. High 13.375 in. Deep

Section 3
APPLICATIONS AND CONFIGURATION

3.1 OVERVIEW

This section contains information to help plan installation of the SC7000 Disk Controller subsystem. Using a few minutes to plan the configuration of the subsystem application can result in a smoother installation with less system-down time. As a planning tool, this section describes some practical matters that should be understood before installation begins.

This section includes application examples and configuration procedures, and is divided into five subsections, as listed in the following table:

Subsection	Title
3.1	Overview
3.2	Application Examples
3.3	Configuration Defined
3.4	Configuration Aids
3.5	Optimizing Performance

Using the information in this subsection should ensure optimum performance from the SC7000 Disk Controller subsystem. A simplified diagram of a typical system hook-up is shown in Figure 3-1.

3.2 APPLICATION EXAMPLES

The SC7000 Disk Controller is designed to interface with DEC VAX-11/750 and VAX-11/780 CPUs and with up to four physical disk drives that use SMD interfacing.

3.2.1 CMI

The CMI with the VAX-11/750 CPU is an interface established by installing the SC7000 Disk Controller directly in slot seven, eight or nine (slot nine preferred for easiest installation) of the CPU backplane.

3.2.2 VMI/SBI

The V-MASTER provides an SBI-type interface with the VMI so that quadwords may be made from longwords, and vice versa.

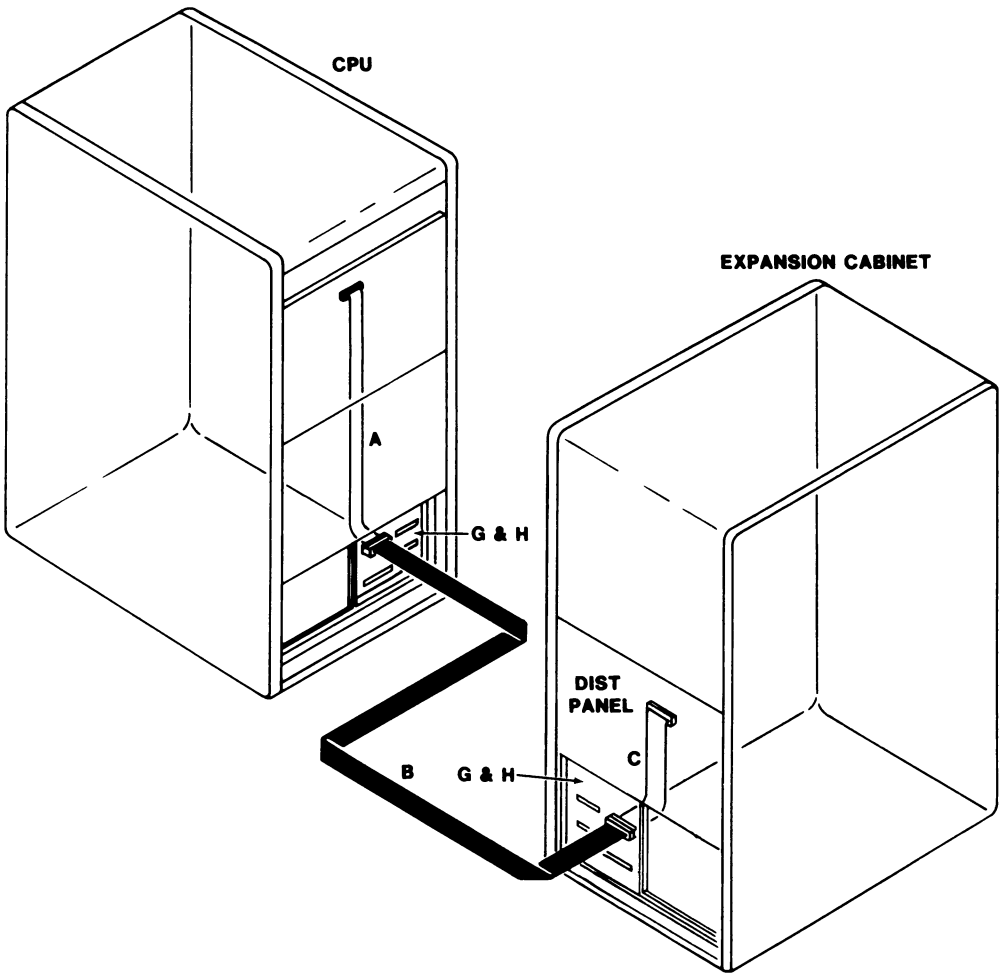


Figure 3-1. Typical System Hook-up

3.2.3 EMULATIONS AND ADVANTAGES

The SC7000 Disk Controller can be used in the VAX-11/750 CPU system or in the VAX-11/780 CPU system.

When it is used in the VAX-11/750 CPU system, it emulates a DEC RH750 Massbus Adapter (MBA) and up to eight RM-type logical disk drives which can be mapped on up to four physical disk drives that have an SMD interface. The SC7000 Disk Controller occupies one of three slots in the VAX-11/750 backplane, which are otherwise dedicated for RH750s. Therefore, the VAX-11/750 can support up to three SC7000 Disk Controllers; one each in slots seven, eight, or nine.

When the SC7000 Disk Controller is used in the VAX-11/780 CPU system, it emulates a DEC RH780 MBA and up to eight logical RM-type disk drives which can be mapped on up to four physical disk drives that have an SMD interface. In the VAX-11/780 CPU system, however, the SC7000 is not mounted directly in the CPU backplane. Instead, it is mounted in an Emulex V-MASTER card cage assembly. The V-MASTER interfaces with the Synchronous Backplane Interconnect (SBI) bus and is mounted in the VAX-11/780 CPU where its application provides important advantages:

- The V-MASTER has only four slots. Two of these slots are for mounting two controllers that functionally use the SBI interface.
- The controllers in the V-MASTER may be the TC7000 Tape Coupler, or the SC7000, SC780, or SC788 Disk Controllers in any combination.
- Any of these controllers functionally emulates one RH780 which contains six slots for mounting PCBAs; therefore, the V-MASTER (with only four slots) can replace two RH780s (12 slots) and support as many logical disk drives as two RH780s.

The SC7000 Disk Controller can be used as a spare for both the VAX-11/750 and VAX-11/780 CPU systems. By setting DIP switches, it can be easily and rapidly reconfigured to match the individual needs of either the VAX-11/750 or VAX-11/780 CPU system in just a few seconds (see Appendix A).

3.2.4 SUPPORTED DISK DRIVES

The SC7000 Disk Controller can support many different models of physical disk drives that have SMD interfaces. Currently supported disk drive models are listed in Appendix A, Table A-1.

3.3 CONFIGURATION DEFINED

In the computer industry, the term **configuration** generally means the physical and logical arrangement of system components, and the

manner in which those components relate to each other. Therefore, the term **configuration** has many possible inferences:

- Size (capacity, speed, data density)
- Cabling (what is connected together)
- Logical arrangement (which functions are combined on which components)
- Location (bus slot, local/remote, bus address, interrupt vector address, unit address),

and so on.

These factors can be established by the user by using switches. Thus, the system configuration and function of a system is defined and determined by the user. With the SC7000 Disk Controller, up to 64 different configurations for standard, expanded, mapped, or multiple RM-type disk drive emulations can be selected by the user (see Appendix A, Table A-2).

3.4 CONFIGURATION DEVICES

Configuration is established by means of connectors, switches, PROMs, indicators, and jumpers.

3.4.1 CONTROLLER CONNECTORS

Connectors J1 and J2 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in Normal operations.

3.4.2 V-MASTER CONNECTORS

The SBI enters the V-MASTER backplane via header connectors J7 through J12 on the right-side edge of the backplane and exits via header connectors J1 through J6 on the left-side edge of the backplane. Pin/signal assignments for the VMI and SBI are listed in Section 8.

The two sets of header connectors on the V-MASTER backplane, associated with slots three and four, are for interfacing the Cable Paddleboard PCBAs with the SC7000 Disk Controller.

Connectors J13 and J14 are both used to carry -5.2Vdc to or from the V-MASTER. Connector J15 connects the AC/DC Low harness to the V-MASTER. B-plus and ground are provided by using the two sets of studs below the J13, J14, and J15 connectors.

3.4.3 SWITCHES

The Bus Interface PCBA has one DIP switch; SW1, which is used to select the TR number for the NEXUS (see subsection 4.5.2.1).

The Bus Translator PCBA has one DIP switch; SW1, which is used to enable/disable early transfer request (TR) and continuous Clock generation (see subsection 4.5.2.2).

The SC7000 Disk Controller contains four 6-pole DIP switches for selection of disk drive emulations; one DIP switch for each of up to four physical disk drives. Two 8-pole DIP switches and two 4-pole DIP switches are also provided for special options (see subsection 4.4.2.5).

3.4.4 PROMS

The Bus Interface PCBA has two control PROMs, 591 and 592, mounted in IC sockets U76 and U78.

The SC7000 Disk Controller PCBA has eight IC sockets for mounting PROMs; six are used for the control memory and are located near the front edge of the PCBA below DIP switches SW1 -- SW4. The IC sockets for the PROMs are reference designated PROM0 through PROM5. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the IC sockets, the ID numbers are placed in the same sequence as the PROM numbers beside each PROM IC socket on the PCBA. The disk drive configuration PROM is located in IC socket U19. An additional PROM in IC socket U126 is used to control buffer addressing.

3.4.5 INDICATORS

Two light emitting diode (LED) indicators are mounted near the front edge of the SC7000 Disk Controller PCBA. They provide the following indications:

FAULT - Steady illumination indicates unsuccessful Self-Test execution.

Regular flashing indicates successful Self-Test but disk drive(s) are not connected to system, or if connected, are not powered up.

Regular flashing during bootstrap operation or during run of microdiagnostic test program indicates continuous Clock not being generated (SW1-3 on Bus Translator PCBA is ON).

Slow flashing indicates two disk drives assigned same unit select number.

FAULT (cont'd) Extinguished indicates successful Self-Test with disk drives connected and powered up.

ACTIVITY - When lit, indicates Write or Read activity is occurring on a selected disk drive.

Extinguished indicates no Write or Read operation is occuring on any disk drive.

3.4.6 JUMPERS

The SC7000 Disk Controller has seven jumper posts. All of them should be open except for F-G, which should be closed. No configuration of these jumpers is required since the SC7000 PCBA is shipped already configured for proper operation. However, there are also jumpers on the VAX-11/750 backplane or on the backplane of the RH780s (see subsections 4.4.1 and 4.5.1). Proper arrangement of these jumpers must be considered when preparing the respective VAX system to operate with the SC7000 Disk Controller.

3.5 OPTIMIZING PERFORMANCE

To verify proper operation and to optimize system performance, the system should be checked for the following conditions:

a. DEC Field Change Order (FCO) number RH750-R0001 incorporated in RH750 (see subsection 4.4.1.2).

b. Index and Sector signals on B-Cable (see subsections 4.3.4 and 4.4.2.4, and Appendix B).

c. Proper noise-suppression provided (see subsection 4.7).

d. System jumpers properly placed (see subsections 4.4.1 and 4.5.1).

e. Proper termination (see subsection 4.5.3.5).

f. SBI headers in proper position (see subsection 4.6.4). If not correctly positioned, VAX-11/780 system cannot function and no optimization is provided.

4.1 OVERVIEW

This section describes the step-by-step procedure for installation of the SC7000 Disk Controller in a VAX-11/750 or VAX-11/780 CPU system. To serve as an outline for the procedure, this section is divided into eight subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	Disk Drive Preparation
4.4	VAX-11/750 System
4.5	VAX-11/780 System
4.6	Backplane Cabling
4.7	Cable Routing and RFI Suppression
4.8	Testing

All steps in these procedures apply to all installations and applications, except for the differences in VAX-11/750 and VAX-11/780 procedures. **Emulex recommends this section be read in its entirety before installation procedures are begun.**

4.1.1 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the SC7000 Disk Controller PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI).

Each SC7000 Disk Controller PCBA is a standalone unit that complies with FCC regulations and is designed to be embedded in a VAX-11/750 CPU cabinet or in a V-MASTER/780 card cage assembly which in turn is embedded in a VAX-11/780 CPU cabinet. When properly installed, the SC7000 Disk Controller system does not cause compliant computers to exceed RFI limits for Class A equipment.

There are two possible configurations in which the SC7000 Disk Controller system can be installed:

a. In the same cabinet as the DEC CPU.

b. In an expansion cabinet that is separate from the CPU cabinet.

To limit radiated RFI, DEC completely encloses the computer system components, that could radiate or conduct RFI, with a grounded metal shield. When installing system components, do nothing that could reduce the effectiveness of the shield. That is, when installation of the SC7000 Disk Controller system [SC7000 Disk Controller PCBAs, Cable Paddleboard PCBAs, Personality Panels, Blank Panels (if any), Bulkhead Distribution Panels (if any), disk drives, and shielded cables] is complete, no gap in the shielding that would allow RFI radiation or conduction can be allowed.

Conducted RFI is generally prevented by installing a filter in the ac line between the computer system and the ac source. Most power distribution panels of current manufacture contain suitable filters.

The procedures required to maintain shield integrity and to limit radiated and conducted RFI are explained fully in subsection 4.7.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the system, visually inspect all assemblies for bent or broken connector pins, damaged components, or other visual evidence of physical damage or incomplete assembly such as missing hardware. The PROMs should be carefully examined to ensure each is firmly and completely seated in its proper socket. Verify that unit model or part number designation, revision level, and serial number agree with those on the shipping invoice. This verification is important to confirm warranty. If evidence of physical damage, missing parts, or identity mismatch is found, notify an Emulex representative immediately.

4.3 DISK DRIVE PREPARATION

Unpack and install the disk drives as instructed in the manufacturer's manual. Position and level them in their final places before beginning installation of the SC7000 Disk Controller. This positioning allows I/O cable routing and length requirements to be accurately determined. To simplify installation and minimize I/O cable length, disk drives should be in a vertical stack or side-by-side.

4.3.1 LOCAL/REMOTE

The LOCAL/REMOTE switch controls whether the disk drive can be powered up from the disk drive front panel (local) or from the SC7000 Disk Controller (remote). Place the switch in the REMOTE position. With the CPU powered down, press the START switch on the front panel of each disk drive; the LED in the START pushbutton/indicator on the operator control panel (OCP) of the disk drive should illuminate but the disk drive should not spin-up and become ready until the CPU is powered up. When the CPU is powered up, the disk drives should spin-up sequentially. This sequential spin-up prevents the heavy current drain that would otherwise be caused if all the disk drives were powered up at the same time. When in the Remote mode, the disk drives power down when the CPU is powered down. While the CPU is powered on, the disk drives may be powered up and powered down individually (to change disk media, for example) by using the START switch on the OCP of the disk drive.

4.3.2 SECTORING

When using disk drives that allow the emulation to produce a one-to-one correspondence between the physical and logical (that is, emulated) recording heads, the disk drives are typically configured for 32 sectors per track.

When the physical disk drive has a different number of heads than the emulated RM-type disk drive, there is no one-to-one correspondence between the physical and logical heads. To accomplish this relationship, the SC7000 Disk Controller operates in a Mapped Track and Cylinder mode.

The disk drives must be hard sectored (see Appendix A, Table A-1, Sectors column) for the number of sectors required by the configuration.

NOTE

> This hard sectoring sometimes results in a short (runt) sector at the end of the track. This runt sector has no adverse affect on the SC7000 Disk Controller, and is sometimes used to do a head change without missing a disk revolution. The Fujitsu Eagle, in the 48 sectors/track mode, requires the runt sector for proper operation.

Because the procedure for entering the sector numbers differs from disk drive model to disk drive model, consult the installation section of the technical manual supplied by the disk drive manufacturer.

NOTE

For information about sectoring the CDC and Fujitsu 2351A models, see Appendix A, subsection A.2.3.

4.3.3 DISK DRIVE NUMBERING

An address from zero to three must be selected for each disk drive. No two disk drives should have the same number. Disk drive addresses are selected by means of an identification (ID) plug or by means of switches on one of the logic PCBAs on the physical disk drive. For the exact disk drive numbering procedure, consult the installation section of the technical manual supplied by the disk drive manufacturer. Option switch SW7-2 allows the disk drives to be numbered from 4 to 7 instead of from 0 to 3, respectively. This feature is sometimes used when dual-porting disk drives to an eight-disk drive controller, such as the Emulex SC788/B1 Disk Controller.

4.3.4 SECTOR AND INDEX MODIFICATIONS

The SC7000 Disk Controller is designed to receive the Sector and Index signals from each disk drive via the B-Cable (see subsection 4.4.2.4). Depending on the disk drive, the Index and Sector pulse signals may be carried on the A-Cable instead of the B-Cable, but for most models, these signals are easily moved to the B-Cable by minor rewiring of the disk drive backplane, or the B-Cable configuration may be ordered from the disk drive manufacturer.

The procedure for moving the Sector and Index signals from the A-Cable to the B-Cable for several of the more common disk drive models is described in Appendix B. If the procedure for the disk drive in question is not detailed in Appendix B, it is usually described in the disk drive technical manual.

NOTE

To prevent significant performance degradation when using more than one disk drive, Emulex strongly recommends modifying the disk drive to place the Sector and Index signals on the B-Cable if the disk drive is not delivered in that configuration.

4.4 VAX-11/750 SYSTEM

Installing the SC7000 Disk Controller in the VAX-11/750 system involves CPU preparation, controller configuration, and controller installation.

4.4.1 VAX-11/750 SYSTEM PREPARATION

Power down the system by placing the main AC circuit breaker at the rear of the CPU cabinet in the OFF position. The AC indicator lamp should remain lit. Open the front door of the CPU cabinet and remove the card-rack cover. Open the rear door of the CPU cabinet and remove the backplane cover. The interior of the CPU cabinet is then accessible to the user.

4.4.1.1 Bus Grant Jumper Removal

To remove applicable Bus Grant jumpers from the CPU backplane, see Figure 4-1 and use the following procedure:

a. Locate Bus Grant jumpers for option slots seven, eight and nine on CPU backplane.

b. Remove Bus Grant jumpers from slot in which SC7000 Disk Controller is to be installed.

c. If a controller is already present in one of the option slots, the Bus Grant jumpers for that slot should already have been removed; if not removed, remove them now.

d. Save removed Bus Grant jumpers.

4.4.1.2 RH750 MBA Reconfiguration

If a DEC RH750 Massbus Adapter (MBA) is presently installed in slot nine of the CPU backplane, Emulex recommends moving the RH750 to slot seven or eight. CMI Bus addressing is not related to the slot in which the SC7000 Disk Controller is installed, so the RH750 can continue to be the bootstrap device, if desired.

If the RH750 is not installed in slot nine, there is no need to move it. It may be necessary, however, to select a different bus arbitration level if the Field Change Order (FCO) described in the following paragraphs has not been installed.

Before removing the RH750 from the card rack in the CPU, determine if FCO #RH750-R0001 has or has not been installed. If the FCO has been installed, revision number A1 should be indicated by Brady markers on the handle of the RH750 module (outside edge of PCBA). Check the ECO/FCO section of the Site Management Guide for the VAX-11/750 CPU to determine if a record of the FCO installation has or has not been entered. Installing the modification provided by this FCO cures the tendency of the RH750 to assert its Arbitration signal for extended periods and thus seize and hold the CMI bus. If this FCO is not installed, other Massbus devices with lower arbitration levels are compelled to generate Data Late error signals. Emulex strongly recommends that FCO #RH750-R0001 be installed before a second Massbus device, such as the SC7000 Disk Controller, is installed in the system.

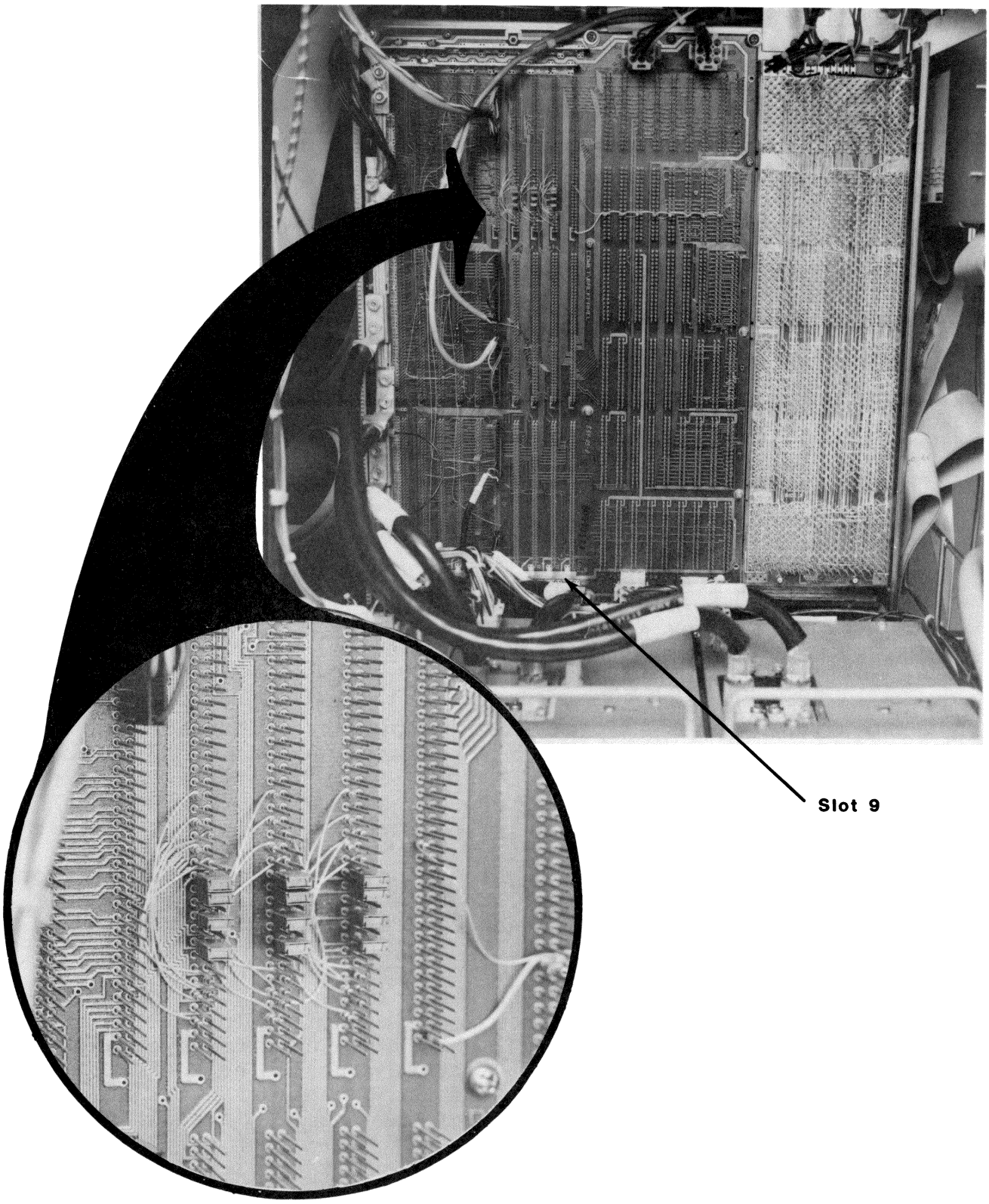


Figure 4-1. VAX-11/750 CPU Backplane with Bus Grant Jumpers

If the FCO cannot be installed before the SC7000 Disk Controller is installed, then to prevent Data Late error signals from the SC7000 Disk Controller, the RH750 must be reconfigured to have a CMI Bus arbitration level lower than that of the SC7000 Disk Controller (see subsection 4.4.1.2.2).

Regardless of whether the FCO has or has not been installed on the RH750, each Massbus device (including the SC7000 Disk Controller -- see subsection 4.4.2.2 or 4.5.2.1.1, as applicable) must be assigned a unique CMI Bus arbitration level.

4.4.1.2.1 RH750 MBA Relocation. Remove the RH750 from slot nine. If modification of FCO #RH750-R0001 has not been installed, it should be installed at this time. Insert RH750 in slot eight or seven.

4.4.1.2.2 RH750 MBA Backplane Reconfiguration. To reconfigure the backplane of the slot in which the RH750 is installed, see Figure 4-2 and use the following procedure:

a. Record jumper arrangement, then remove the following jumpers from slot nine:

   SLOW CMI EN H
   MBA SELECT 0
   MBA SELECT 1
   CMI ARBITRATION (ARB) LEVEL

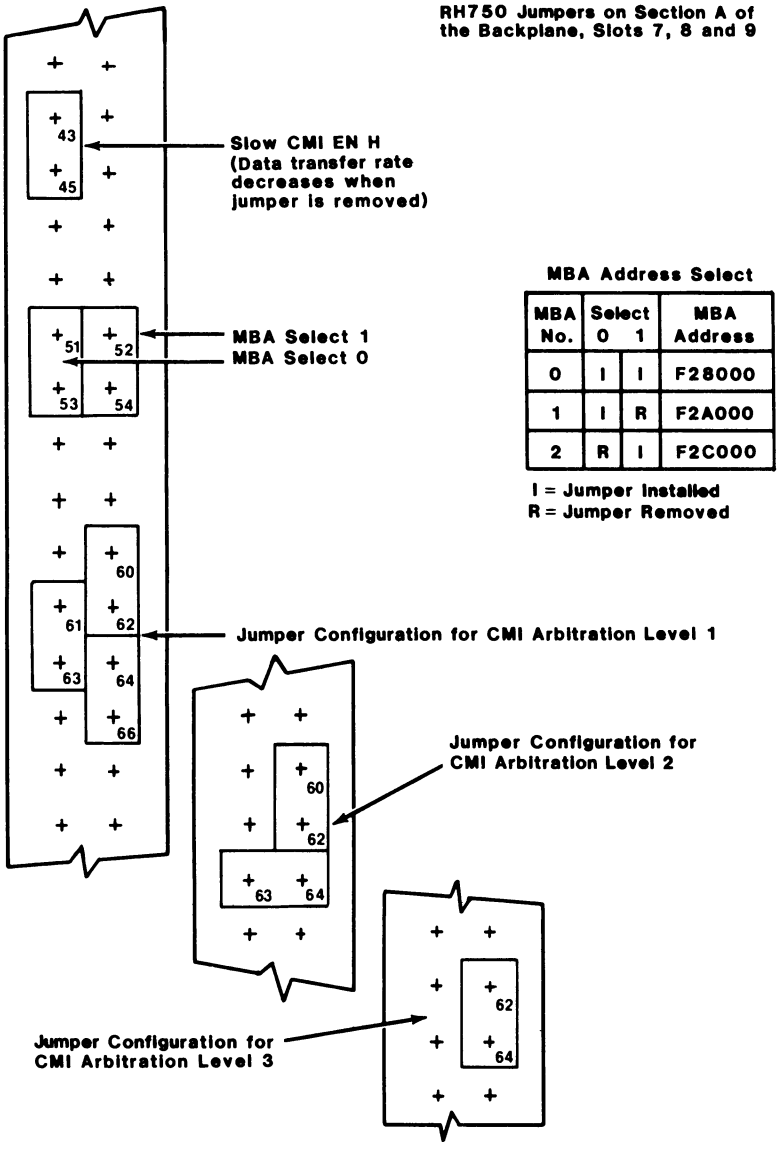
b. Place SLOW CMI EN H jumper in same relative location on CPU backplane of new slot for RH750.

c. If RH750 is to remain Bootstrap device (address F28000), place both MBA SELECT jumpers in same relative location on CPU backplane of new slot for RH750. If SC7000 Disk Controller is to be Bootstrap device, select either F2A000 or F2C000 as MBA address for RH750 (see table in Figure 4-2).

d. Determine CMI ARB level assigned to original RH750 MBA installation (use record from step a and see Figure 4-2).

e. If FCO #RH750-R0001 has been installed and RH750 is to remain Bootstrap device, place CMI ARB jumpers in same relative location on backplane of RH750 slot.

f. If FCO #RH750-R0001 has not been installed and CMI ARB level three had been assigned, connect jumper to select a lower CMI ARB level (two or one). This step must be performed whether RH750 MBA is or is not moved. Removed Bus Grant jumpers (see subsection 4.4.1.1) should be used to select lower CMI ARB level.



MBA No.	Select 0	Select 1	MBA Address
0	I	I	F28000
1	I	R	F2A000
2	R	I	F2C000

Figure 4-2. Backplane Jumpers for RH750

g. Record location, then remove three Massbus plugs from sections B and C of backplane slot in which RH750 is installed and temporarily set them on top of card cage in CPU.

h. After A-Cable and B-Cables have been installed on Cable Paddleboard PCBA for SC7000 Disk Controller, plug Massbus plugs, removed in step g, into same relative location on new backplane slot for RM750.

4.4.1.3 Bootstrap ROM Installation

The Bootstrap ROMs for the VAX-11/750 CPU are located on the L0016 Memory Controller PCBA shown in Figure 4-3. These ROMs are plugged into IC sockets so that they can be easily removed and/or replaced. DEC factory placement of the Bootstrap ROMs is listed in Table 4-1.

Table 4-1. DEC Factory Placement of Bootstrap ROMs

Bootstrap Switch Position	Device Type
A	TU58
B	RL02
C	RK07
D	EMPTY

When installing an SC7000 Disk Controller system, a Massbus Disk Bootstrap ROM (Emulex P/N 497) must be installed on the L0016 Memory Controller PCBA. This ROM is installed in spare IC socket U8 before the SC7000 Disk Controller is shipped from the factory. Carefully remove the Bootstrap ROM from IC socket U8 and plug it into the appropriate socket on the Memory Controller. Normally the Massbus Disk Bootstrap ROM497 is plugged into the IC socket, on the L0016 Memory Controller PCBA, which correlates to Bootstrap switch position D; but the user can rearrange the Bootstrap ROM locations to have any Bootstrap switch-position configuration. The only configuration restriction is that the TU58 Bootstrap ROM remain on the L0016 Memory Controller PCBA, preferably in IC socket for Bootstrap switch position A or D (see Figure 4-3). Note that the physical location of the sockets may be different on older L0011 memory boards.

4.4.2 SC7000 CONFIGURATION IN VAX-11/750 CPU

Selection of the Base Address and arbitration level for the SC7000 Disk Controller is done via DIP switch SW8. Component locations on the SC7000 Disk Controller are shown in Figure 4-4. The SC7000 Disk Controller must be configured before it is inserted in the CPU chassis. The state of switch SW7-7 defines CPU type; ON (closed) is for VAX-11/780 mode of operation, OFF (open) is for VAX-11/750 mode of operation.

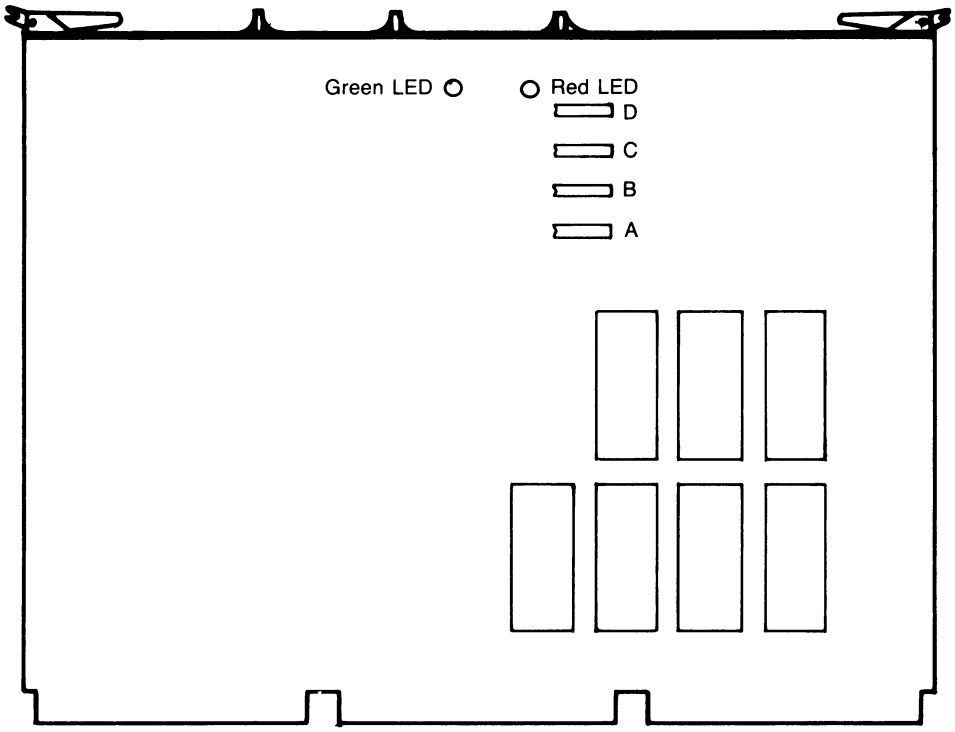


Figure 4-3. L0016 Memory Controller PCBA

4.4.2.1 MBA RH Device Number Selection

The MBA RH Device number designates the CMI Base Address and the Interrupt Vector Address for the SC7000 Disk Controller. The MBA RH Device number is selected by DIP switches SW8-7 and SW8-8. If the disk drive that is used to bootstrap the system on power-up is connected to the SC7000 Disk Controller, the Base Address for that controller must be F28000. This selection does not affect the Arbitration level of the SC7000 Disk Controller, which is established as described in subsection 4.4.2.2. Switch positions for selection of the MBA RH Device number are listed in Table 4-2.

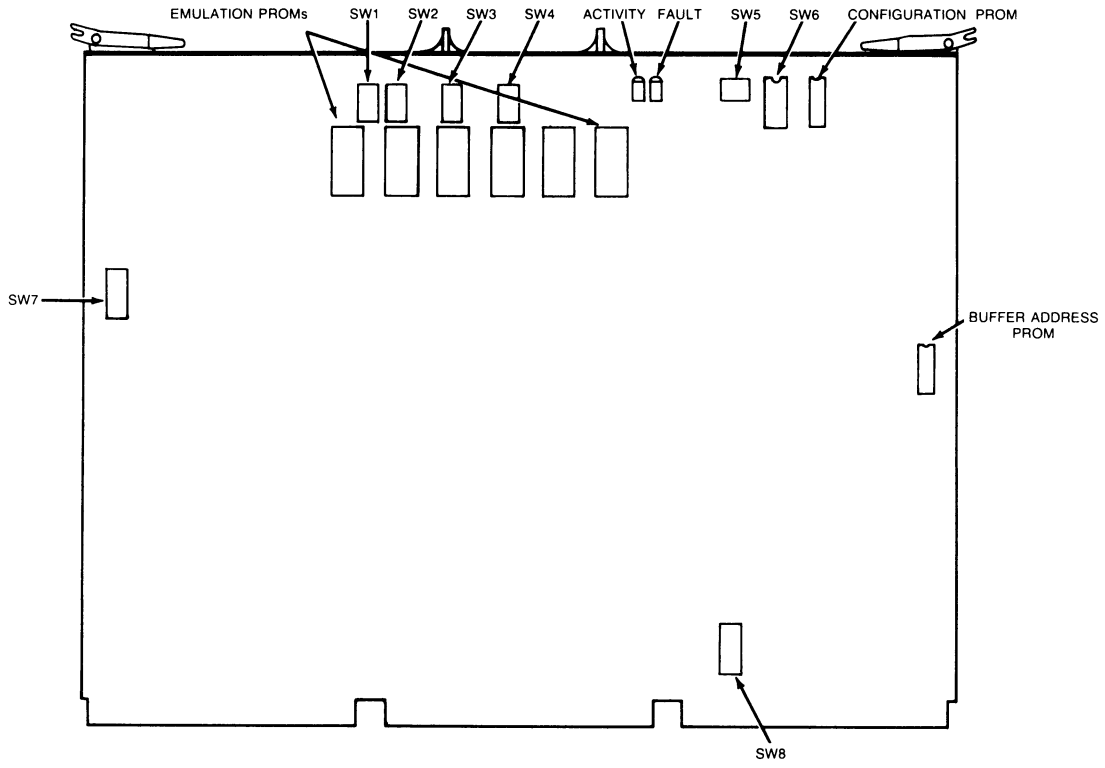


Figure 4-4. SC7000 Disk Controller PCBA, Component Locations

Table 4-2. Switch Settings for Base Address, Interrupt Vector Address and MBA RH Device Number

SW8-7	SW8-8	Base Address	Interrupt Vector Address	RH Device Number
O	O	F28000	150	RH0
O	C	F2A000	154	RH1
C	O	F2C000	158	RH2
O = Open		C = Closed		

4.4.2.2 Arbitration Level Selection

The Arbitration (Bus Priority) level is selected by DIP switches SW8-2 through SW8-6, as listed in Table 4-3. Each Massbus device must be assigned a unique arbitration level. If an RH750 is already installed in the system and the jumpers on the CPU backplane for that device have not been inspected to determine its arbitration level, do so now (see Figure 4-2). If the DEC FCO has been installed, select any Arbitration level that is not being used. If the DEC FCO has not been installed, select a higher Arbitration level (see subsection 4.4.1.2).

Table 4-3. Arbitration Level Selection

Arbitration Level	SW8- 2	3	4	5	6	Bus Priority
3	C	O	O	O	O	Highest MBA level
2	O	C	O	C	O	
1	O	O	C	C	C	Lowest MBA level
O = Open			C = Closed			

4.4.2.3 Disk Drive Configuration Selection

The phrase "disk drive configuration selection" describes the process used to select the logical disk drive units that are to be emulated by the SC7000 Disk Controller when a particular set of physical disk drives is used. By using those logical disk drive units with the SC7000 Disk Controller, a specific type and arrangement of DEC subsystems can be emulated. Each emulated subsystem is a logical disk drive unit. DIP switches SWn-1 through SWn-6 (where SWn is SW1, SW2, SW3 or SW4, as applicable) allow the user to select the logical disk drive unit configuration, which is limited only by the physical disk drives available in the system. The configuration table, and instructions for using it, are in Appendix A.

4.4.2.4 Index and Sector Pulse Signal Selection

The SC7000 Disk Controller is designed to have the Index and Sector pulse signals on the B-Cable from each physical disk drive. These signals are necessary for proper operation of the sector counters associated with each disk drive. The RM emulations require an updated sector counter whose content can be read by the VAX-11/750 and VAX-11/780 CPUs. Failure to have a valid sector counter may cause incorrect operation of the software that is responsible for sensing the rotational position of the disks.

The SC7000 Disk Controller can operate with the Index and Sector pulse signals on the A-Cable, instead of the preferred B-Cable. if DIP switch SW7-8 on the SC7000 Disk Controller PCBA is placed in the ON (CLOSED) position. This feature is useful for initial evaluation of the SC7000 Disk Controller when operating with a disk drive that provides Index and Sector pulse signals only on the A-Cable. When operating in this configuration, however, there is a substantial loss of system capabilities and performance; e.g., the Search command operates as a Seek command, the sector count in register RMLA is incorrect, each Data Transfer operation must wait for an Index pulse signal to synchronize the sector counter, and some of the lower-level diagnostics produce some unnecessary errors. Emulex strongly recommends that disk drives delivered with the Index and Sector pulse signals on the A-Cable be modified to place those signals on the B-Cable before the disk drives are used

in the system. Modification instructions for some disk drives are in Appendix B.

4.4.2.5 Option Switches

A separate, unique DIP switch is provided for each of four physical disk drives that can be included in the system. These DIP switches are located at the left-center front edge of the SC7000 Disk Controller PCBA (see Figure 4-4). DIP switch SW1 selects a hexadecimal number that represents the configuration for physical disk drive unit 0. Switch SW2 selects a hexadecimal number that represents the configuration for physical disk drive unit 1. Switch SW3 selects a hexadecimal number that represents the configuration for physical disk drive unit 2. Switch SW4 selects a hexadecimal number that represents the configuration for physical disk drive unit 3. Thus, the user must set the appropriate disk drive configuration hexadecimal number in each of the four DIP switches to configure the entire SC7000 Disk Controller for system operation with up to four physical disk drives. Appendix A details configuration numbers for disk drive emulations and switch settings for those configurations.

Several other options are user-selectable by means of DIP switches. The functions of the switches that select those options are listed and defined in Tables 4-4, 4-5, and 4-6.

Table 4-4. Option Switches SW5 and SW6 Settings

Option Switch	Open	Closed	Function
SW5-1	Run	Halt-Reset	Controller Run/Halt-Reset[1]
SW5-2	Disable	Enable	Dual-Access mode[3]
SW5-3			Not used[2]
SW5-4			Not used[3]
SW6-1			Not used[2]
SW6-2			Not used[2]
SW6-3			Not used[2]
SW6-4			Not used[2]

[1]Causes VAX CPU reset as well when SW8-1 is ON (CLOSED).
[2]Not used switches MUST BE OFF.
[3]See subsection 6.6.5.7.

4.4.2.5.1 Dual-Access Mode. The Dual Access mode is enabled by placing switch SW5-2 in the ON (CLOSED) position. This mode provides compatibility with VMS when the system is configured for Dual Access operation. This mode should be selected only when the disk drive has dual ports and is configured for the Dual Port mode of operation. For information about programming in this mode, see subsection 6.6.5.

Table 4-5. Option Switch SW7 Settings

Option Switch	Open	Closed	Function
SW7-1	---	---	Not used[1]
SW7-2	0-3	4-7	Selects physical disk drive address range
SW7-3	---	---	Not used[1]
SW7-4	Disable	Enable	Delay on overlapped searches to the same physical disk drive[4]
SW7-5	Disable	Enable	CDS Trident disk drive compatibility.
SW7-6	Disable	Enable	Dual-Port mode.
SW7-7	VAX-11/750	VAX-11/780	SC7000 Address mode[2]
SW7-8	B-Cable	A-Cable	Sector and Index signals[3]

[1]All unused switches MUST BE OFF.
[2]Open for VAX-11/750 operation, closed for VAX-11/780 operation.
[3]See subsections 4.3.4 and 4.4.2.4.
[4]See subsection 6.5.5.

4.4.2.5.2 Dual-Port Mode. The Dual Port mode is enabled by placing DIP switch SW7-6 in the ON (CLOSED) position. It should be selected and used only when the system meets the following conditions:

a. Properly written Dual Port Driver software is being used.

b. The disk drive has dual ports and is configured for the Dual Port mode of operation.

Table 4-6. Option Switch SW8 Settings

Option Switch	Open	Closed	Function
SW8-1	Disable	Enable	VAX-11/750 CPU reset (via AC LOW) when SW5-1 is switched ON.
SW8-2			MBA Arbitration Level[1]
SW8-3			MBA Arbitration Level[1]
SW8-4			MBA Arbitration Level[1]
SW8-5			MBA Arbitration Level[1]
SW8-6			MBA Arbitration Level[1]
SW8-7			VAX-11/750: CMI vector/address[2]
SW8-8			VAX-11/750: CMI vector/address[2]

[1]See subsection 4.4.2.1
[2]See subsection 4.4.2.2.

4.4.3 SC7000 INSTALLATION IN VAX-11/750 CPU

The SC7000 Disk Controller PCBA may be installed in slot seven, eight, or nine of the VAX-11/750 CPU cabinet. To make installation of the Cable Paddleboard PCBA easy, slot nine should be used. To install the SC7000 Disk Controller PCBA in the VAX-11/750 CPU cabinet, use the following procedure:

a. Verify CPU power is OFF to avoid possible injury or circuit damage.

b. Position PCBA so that component side faces in same direction as component side of other PCBAs already installed in CPU cabinet.

c. Verify PCBA is properly positioned in throat of each connector before attempting to seat PCBA in connectors.

d. Gently but firmly push extractor handles on PCBA with even pressure until PCBA is fully seated.

NOTE

To remove any PCBA in system, raise extractor handles until handles are erect, then pull PCBA from mounting slot.

4.4.3.1 Cable Paddleboard PCBA Installation in VAX-11/750

One Cable Paddleboard PCBA is required for each SC7000 Disk Controller. In the VAX-11/750 CPU system, the PCBA is installed on the backplane of the slot that is to contain the SC7000 Disk Controller PCBA. This procedure assumes the SC7000 Disk Controller is installed in slot nine and that the referenced view is from the rear and toward the backplane.

An installation kit, Emulex part number TU7513001, is used to install the Cable Paddleboard. To install the Cable Paddleboard PCBA on the VAX-11/750 CPU backplane, see Figures 4-5 and 4-6 and use the following procedure:

a. Verify CPU power is OFF.

b. Remove Phillips-head screw, located to right side of backplane slot 10 between sections B and C.

c. Install support bracket on Cable Paddleboard PCBA.

d. Plug A-Cable and all B-Cables into appropriate connectors on Cable Paddleboard PCBA. These six connectors are on left side of PCBA.

e. Carefully position three connectors on Cable Paddleboard PCBA over backplane connector pins (sections B and C) of slot 10 so that white guide between top and middle connectors is between bottom two pins of section B and top two pins of section C, and at same time rest PCBA against pins at right side of backplane connector. When position of PCBA looks and feels as if backplane pins can properly engage connectors on PCBA, gently push PCBA forward until it bottoms on backplane header.

f. Insert screw, removed in step a, through support bracket and tighten in place.

NOTE

Subsequent Cable Paddleboard PCBAs for up to two additional SC7000 Disk Controllers are attached to the first Cable Paddleboard PCBA with the standoffs in the installation kit.

4.5 VAX-11/780 SYSTEM

Installing the SC7000 Disk Controller in the VAX-11/780 system involves system preparation, V-MASTER preparation, controller configuration, controller installation in the V-MASTER, and V-MASTER installation on the SBI bus.

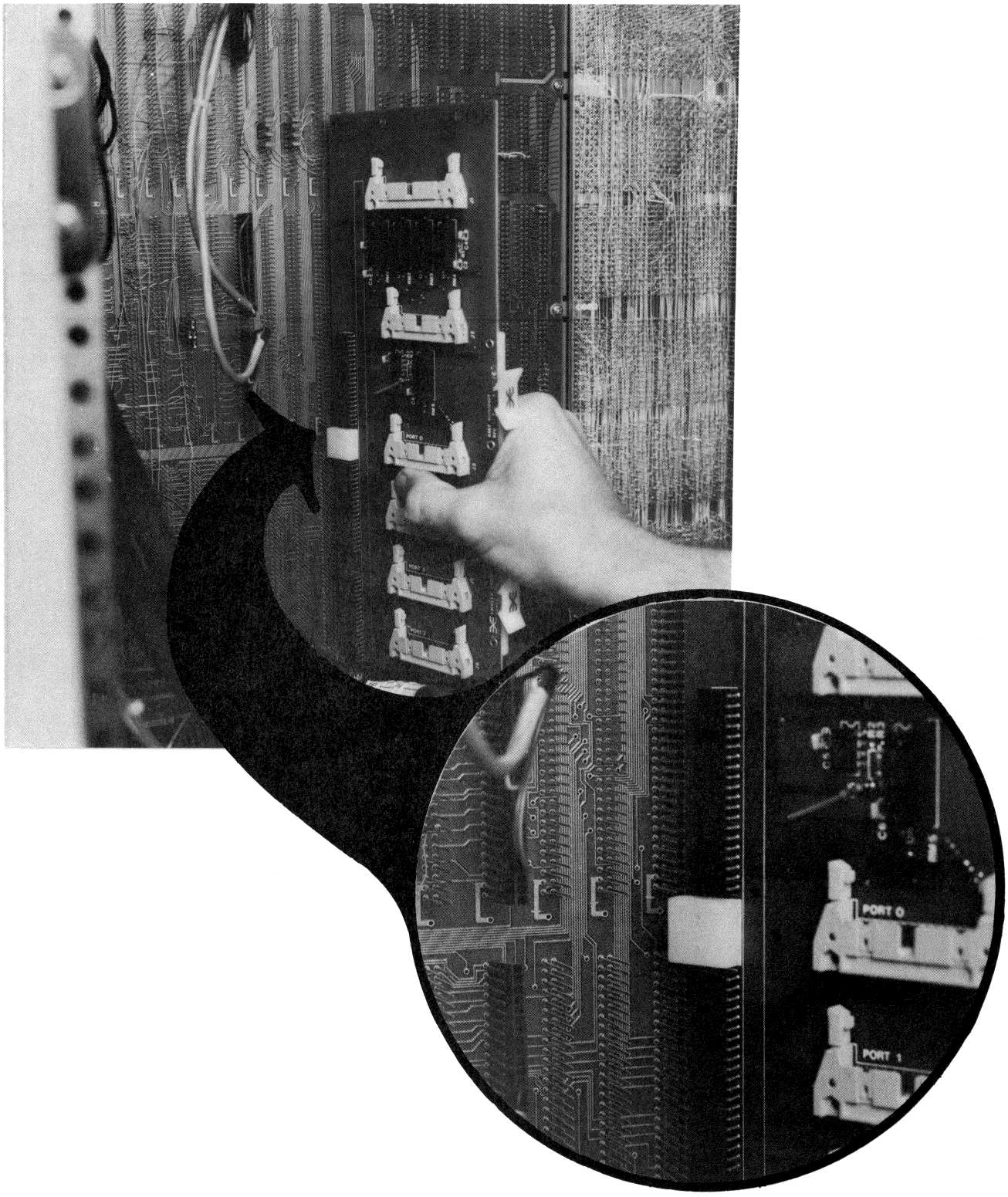
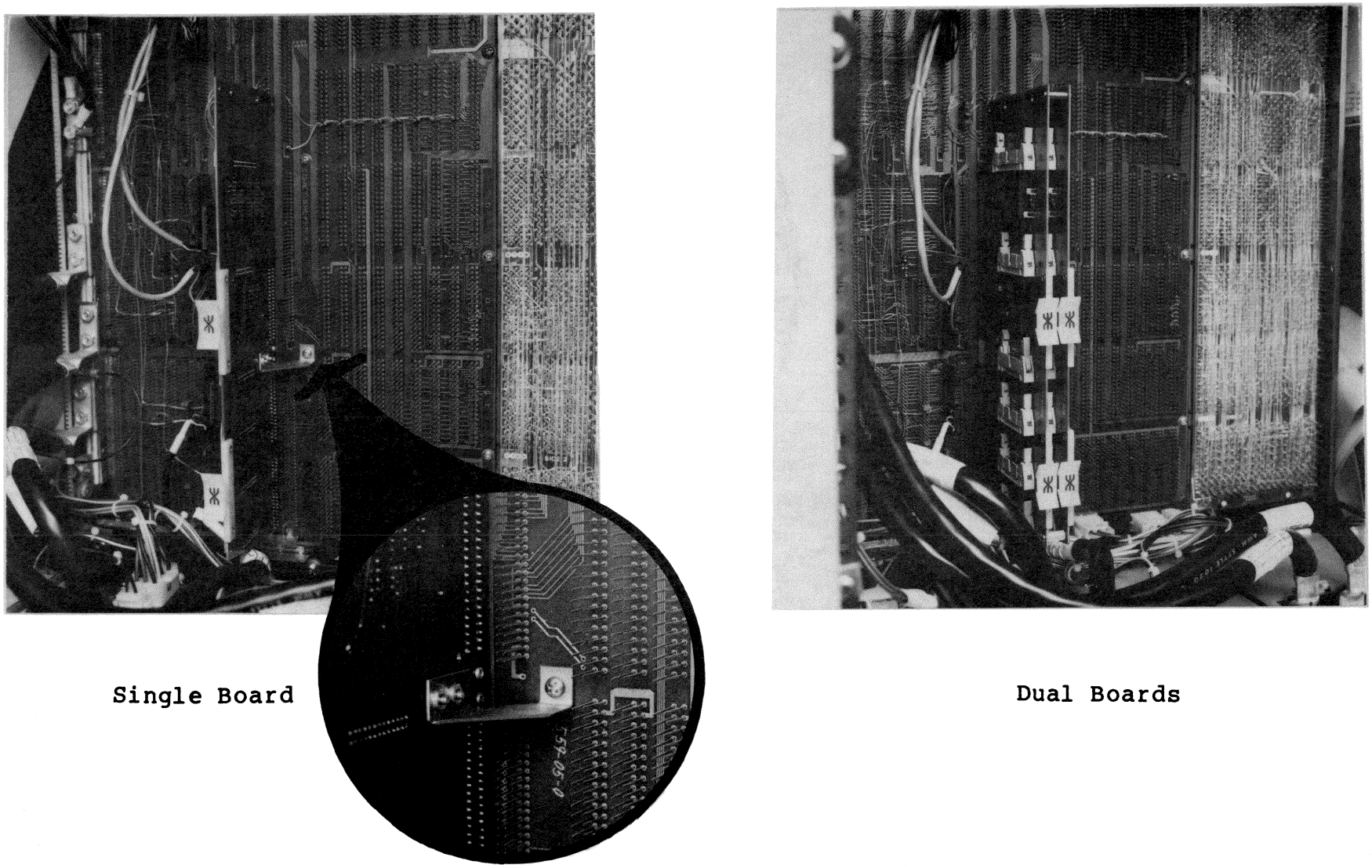


Figure 4-5. Cable Paddleboard PCBA Installation
(stiffener removed for clarity)



Single Board

Dual Boards

Figure 4-6. Single and Dual Paddle Board Mounting

4.5.1 VAX-11/780 SYSTEM PREPARATION

Before installation of an additional NEXUS such as a V-MASTER, DEC MBA, OR DEC UBA, the TR level and address range of all previously installed NEXUSes must be determined to prevent new devices from having the same TR level or addresses which are presently in use.

DEC TR levels are normally associated with the various NEXUS address ranges, as listed in Table 4-7. For DEC MBAs, the TR level and the address range are selected separately.

Table 4-7. Setting Numbers for Base Address

Base Address	TR Level	Setting Number	Base Address	TR Level	Setting Number
20008000	TR4	3	20010000	TR8	7
2000A000	TR5	4	20012000	TR9	8
2000C000	TR6	5	20014000	TR10	9
2000E000	TR7	6	20016000	TR11	10

To determine the Base Address for a particular DEC MBA, a combination of pin/plugs at the top of the DEC MBA chassis backplane is used. The pin/plugs are weighted, starting with the leftmost pair of pins and counting four pairs to the right: eight, four, two, and one. The sum of the pin/plugs equals the setting number for the desired Base Address, as listed in Table 4-7; e.g., if the desired Base Address is 20010000, pin/plugs four, two and one would be installed.

Pins to the right of these four pairs are used to select the Bus Request (BR) level. It is not necessary to determine the BR level of the RH780 MBA or to select a different BR level for the V-MASTER/780.

A jumper wire on the CPU backplane of the second PCBA slot determines the TR level. The different jumper positions are listed in the following table:

F2F1 to F2C1 = TR1		F2F1 to F2J2 = TR7	
F2F1 to F2D1 = TR2		F2F1 to F2M1 = TR8	
F2F1 to F2E1 = TR3		F2F1 to F2N1 = TR9	
F2F1 to F2F2 = TR4		F2F1 to F2P1 = TR10	
F2F1 to F2H2 = TR5		F2F1 to F2P2 = TR11	
F2F1 to F2J1 = TR6		F2F1 to F2S2 = TR12	

The RH780 MBA backplane is shown in Figure 4-7. In this figure, letters are included to help identify pin locations, although the letters are not actually on the RH780 MBA backplane. The numbers on the backplane do not appear in the same location as shown in Figure 4-7; they are located near the center of the PCBA, not directly above block "F".

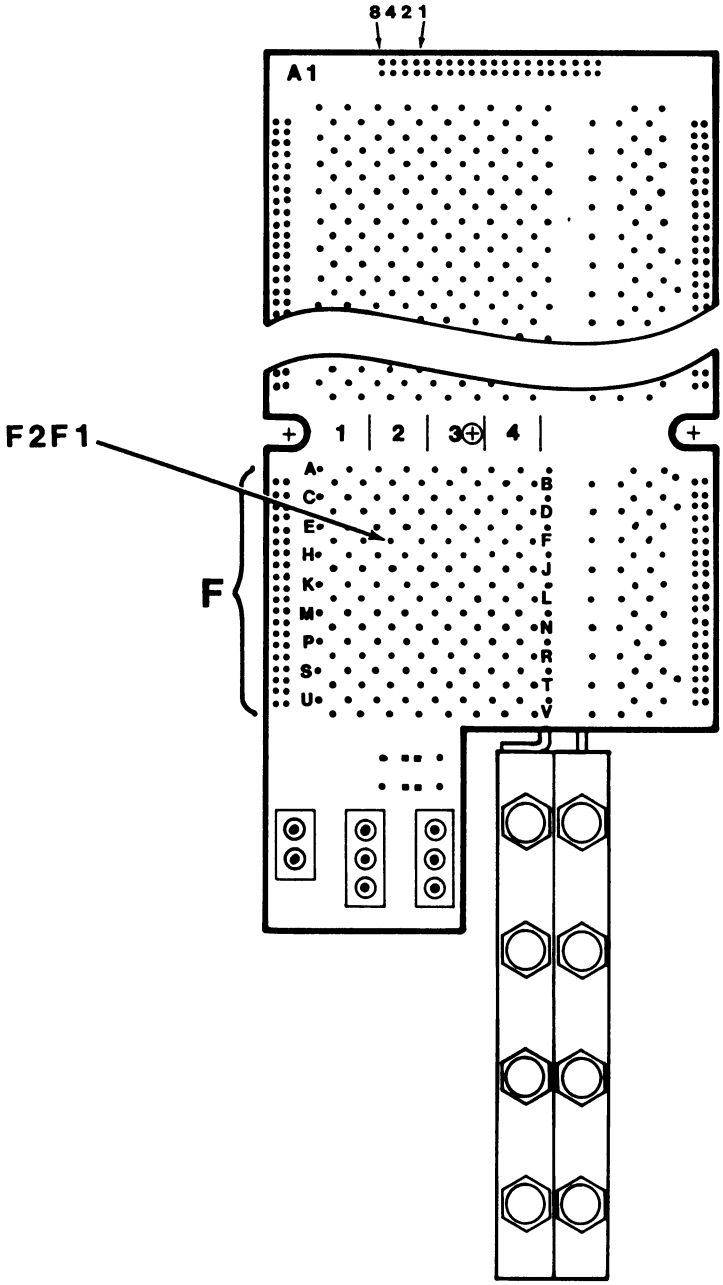


Figure 4-7. RH780 MBA Backplane

Jumper pin locations are defined by a series of numbers and letters which designate block, column and row. The first letter designates the block. The blocks of pins are lettered in sequence, beginning with block "A" at the top and proceeding to block "F" at the bottom (six blocks). The next character in the pin identification code is a number that designates a column which is four pins wide; therefore, the first four pins at the left are in column one. The next character is a letter that designates a row of pins. Each row is labeled in Figure 4-7. The last character is a number that designates which of two pins in the same row is designated by the same column number. A number "1" designates the left-side pin of that column in a particular row, and a number "2" designates the right-side pin. In Figure 4-7, pin F2F1 is indicated by an arrow.

Normally, changing the TR level of an installed DEC RH780 MBA is not necessary; i.e., having the V-MASTER/780 at a lower TR level (TR10 or TR11) is desirable because it has a 12-sector buffer.

4.5.2 V-MASTER PREPARATION

The V-MASTER/780 assembly consists of a wire chassis and an Emulex VMI Bus backplane that can accept four hex-sized PCBAs. Two of the PCBA slots are for the hardware needed to mate the DEC SBI with the Emulex SC7000 Disk Controllers. The Bus Interface PCBA (Emulex P/N SU7810401) and the Bus Translator PCBA (Emulex P/N SU7810402 revision D or later, or P/N SU7810409) are part of the completed V-MASTER/780 assembly. Procedures for configuring these two PCBAs for particular applications are described in the next four subsections. The remaining two hex-sized PCBA slots in the V-MASTER/780 chassis are for installation of two Emulex Controller PCBAs such as the SC780, SC788, SC7000, or TC7000.

* * * * * * *
W A R N I N G
* * * * * * *

TO AVOID POSSIBLE PERSONAL INJURY OR CIRCUIT DAMAGE, **ALWAYS** VERIFY SYSTEM POWER IS **OFF** BEFORE REMOVAL OR REPLACEMENT OF ANY SYSTEM PCBA.

4.5.2.1 Bus Interface PCBA

Each MBA installed in the V_MASTER is a nexus; therefore, each SC7000 Disk Controller is a nexus. Each nexus on the SBI is assigned a transfer request (TR) number which is both the arbitration level and the SBI address of the device. MBA nexuses are generally assigned TR numbers ranging from TR8 through TR11 (the first DEC MBA is usually assigned to TR8). The TR number and the Interrupt Request level for each SC7000 Disk Controller that can be installed in the V-MASTER are selected by setting DIP switches SW1-1 through SW1-6 on the Bus Interface PCBA (P/N SU7810401) as listed in Tables 4-8 and 4-9. DIP switch SW1 is shown in Figure 4-8.

Table 4-8. DIP Switch Settings for TR Level

TR Level	SW1-4	SW1-3	SW1-2	SW1-1
4	O	C	O	O
5	O	C	O	C
6	O	C	C	O
7	O	C	C	C
8	C	O	O	O
9	C	O	O	C
10	C	O	C	O
11	C	O	C	C
O = Open	C = Closed			

Table 4-9. DIP Switch Settings for Interrupt Request Level

Level	SW1-6	SW1-5
4	O	O
5 --Normal Setting--	O	C
6	C	O
7	C	C

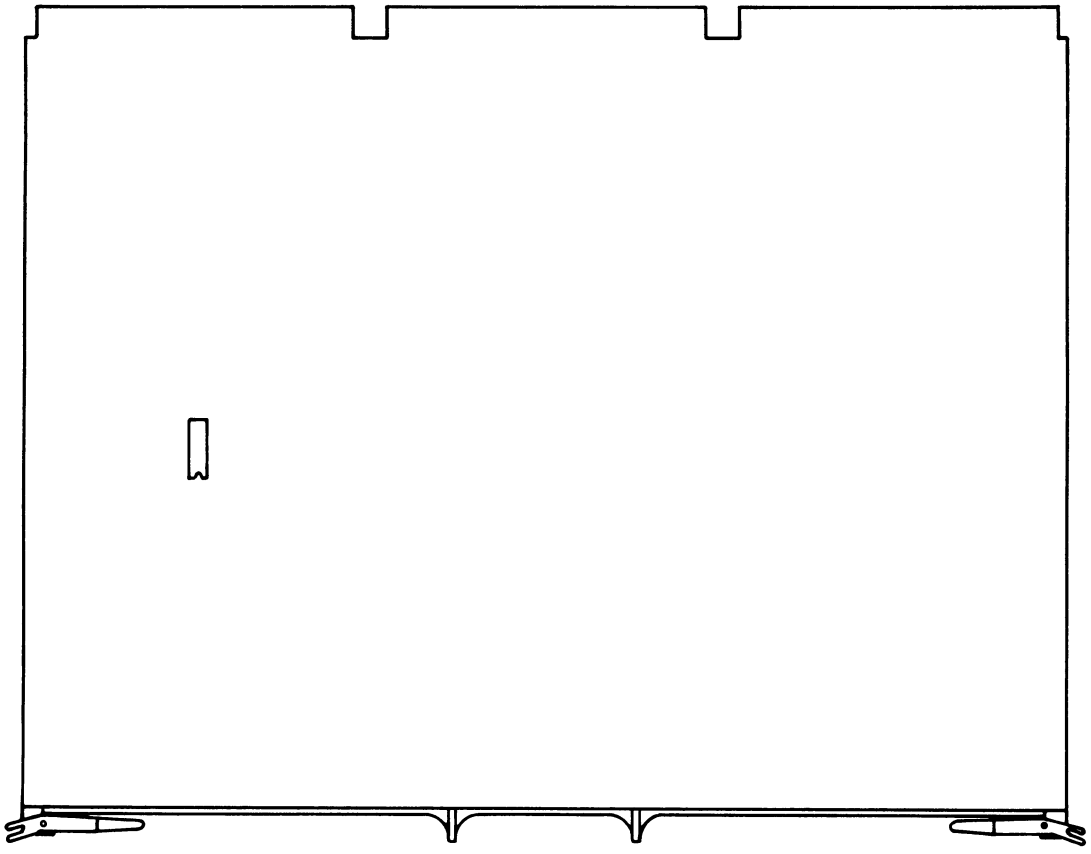


Figure 4-8. Bus Interface PCBA, Component Locations

Access to DIP switch SW1 on the Bus Interface PCBA depends on the V-MASTER location in the system. To gain access to this PCBA, it may be necessary to temporarily remove it by raising its extractor handles and pulling it from its mounting slot.

4.5.2.1.1 SBI Arbitration Level (TR Number). When two SC7000 Disk Controllers are installed in the V-MASTER, the two MBA devices they represent are assigned an even-odd pair of addresses such as TR8 and TR9, or TR10 and TR11. The TR switch settings on the Bus Interface PCBA are made for the even TR number. The controllers are differentiated by the slot they occupy in the V-MASTER; thus, the controller in slot three has the even TR number and the controller in slot four has the odd TR number.

A single SC7000 Disk Controller can be installed in either slot three or four, and can be assigned either an even or an odd TR number.

4.5.2.1.2 SBI Interrupt Request Level. The one or two SC7000 Disk Controllers are assigned Interrupt Request levels by DIP switches SW1-5 and SW1-6 on the Bus Interface PCBA. Normally level five should be used. Switch settings are listed in Table 4-9.

4.5.2.1.3 Bus Interface PCBA Installation. The Bus Interface PCBA is installed in slot one of the V-MASTER/780 chassis; i.e., right-side slot as viewed from front. The Bus Translator PCBA is installed in slot two. Component side of PCBAs should face toward the right (same direction as on other PCBAs installed in system chassis). To reinstall the PCBA after setting DIP switches, carefully insert PCBA in throat of connector slots. Verify PCBA is properly positioned in throat, then seat PCBA by firmly pressing down on extractor handles.

4.5.2.2 Bus Translator PCBA

The Bus Translator PCBA includes piano-type DIP switch SW1 at the front edge, as shown in Figure 4-9. SW1 is accessible without removing the PCBA from the V-MASTER, and it enables selection of two features: Early Transfer Request and Continuous Clock Generation.

- - - - - - -
C A U T I O N
- - - - - - -

For proper operation of the SC7000 Disk Controller, the Bus Translator PCBA **must be** P/N SU7810402 revision D or later, or P/N SU7810409.

4.5.2.2.1 Early Transfer Request. When DIP switches SW1-1 and SW1-2 are placed in the ON (CLOSED) position, early TR arbitration for the SC7000 Disk Controllers in V-MASTER slots three and four, respectively, is enabled. This feature asserts the TR level of the V-MASTER 800 nanoseconds before an SBI Read Data command is issued.

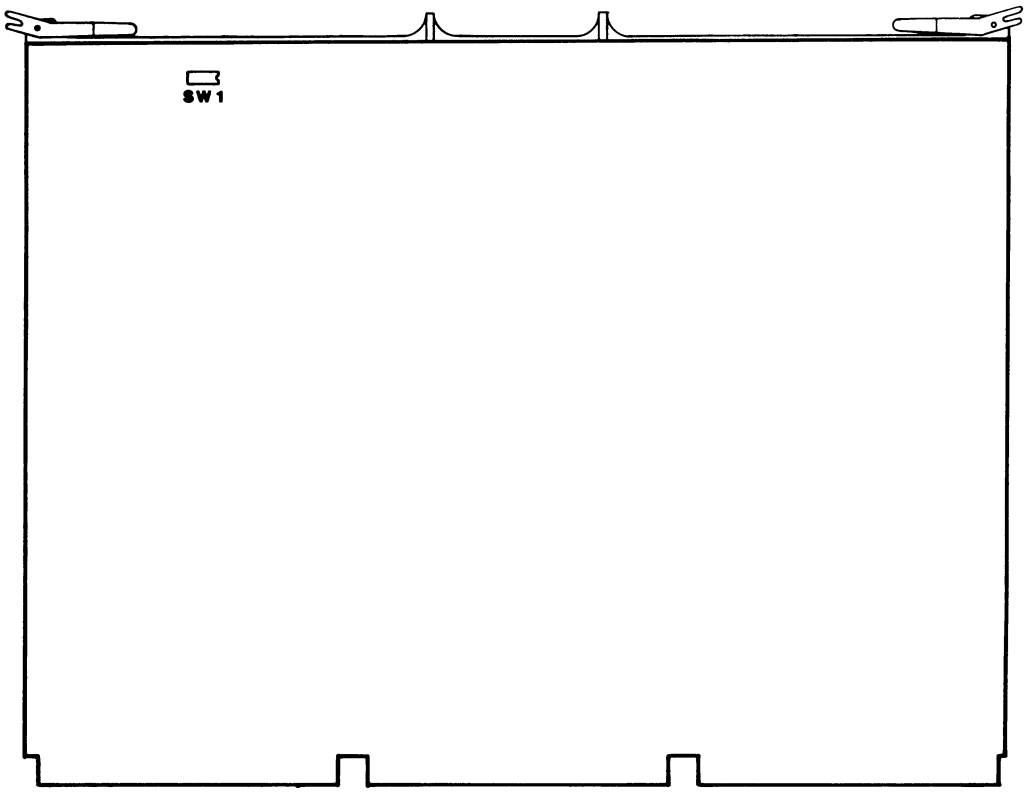


Figure 4-9. Bus Translator PCBA, Component Locations

Early TR assertion prevents any nexus, which has a lower priority than the V-MASTER, from using the SBI bus. If no other nexus with a higher arbitration level requests the SBI bus after the Early TR level of the V-MASTER is asserted, the first in-first out (FIFO) command stack in the VAX Memory Controller empties and immediately responds to the Read Data command from the V-MASTER in the last SBI cycle of this Extended/Early TR operation. Since the CPU is always set for the lowest arbitration level (TR15), a small amount of processing time is lost when this feature is enabled. The amount of time lost depends on the type of VAX Memory Controller installed in the system and on the intensity of CPU or I/O processing. The user should run a benchmark test to determine if this feature is or is not desirable for the system. Early TR arbitration may be useful to users of disk drives that have high data-transfer rates; e.g., the Fujitsu model 2315A Eagle when set for 48 sectors/track.

4.5.2.2.2 Continuous Clock Generation. When DIP switch SW1-3 is placed in the OFF (OPEN) position, continuous Clock generation is enabled for both controllers in the V-MASTER, and the FAULT LED on each controller PCBA remains unlit during a system bootstrap operation, or during the running of micro-diagnostic test programs. When switch SW1-3 is ON (CLOSED), the controllers in the V-MASTER lack continuous Clock generation and the FAULT LED on each controller PCBA blinks during a system bootstrap operation or during the running of micro-diagnostic test programs.

4.5.3 SC7000 CONFIGURATION IN VAX-11/780 CPU

One or two SC7000 Disk Controller PCBAs may be plugged into the V-MASTER/780 assembly. The SC7000 Disk Controllers need to be configured for the particular application. This subsection describes those configuration procedures. Because not all DIP switches on the SC7000 Disk Controller are readily accessible after the SC7000 Disk Controller PCBA is installed in the V-MASTER/780 card cage assembly, configuration should be done before such installation.

4.5.3.1 SC7000 Disk Controller Base Address and Arbitration Level

The Base Address of the SC7000 Disk Controller is selected with respect to the V-MASTER/780 slot in which the SC7000 Disk Controller PCBA is to be installed. The SC7000 Disk Controller must be assigned VMI Arbitration level two or one, depending on the slot in which it is to be installed. Slot three is right-side slot and slot four is left-side slot when viewed from the front of the V-MASTER/780 card cage assembly. DIP switch SW8 is used, as listed in Table 4-10. For single PCBA installations, slot number three should be used because the bracket on the cable adapter is designed for slot three. Slot four also uses a standoff which is mounted to this PCBA after this PCBA has been installed in slot number three.

Table 4-10. DIP Switch Settings for Base Address and VMI Arbitration Level

Controller Position	SW8- 1	2	3	4	5	6	7	8
Slot 3 (R)	C	O	C	O	O	O	O	O
Slot 4 (L)	C	O	O	C	C	O	O	C
O = Open			C = Closed					

NOTE

VMI Arbitration level setting is not related to SBI Arbitration level described in subsection 4.5.2.1.1.

4.5.3.2 Disk Drive Configuration Selection

Disk drive configuration selection for SC7000 Disk Controllers installed in V-MASTER/VAX-11/780 CPU systems is the same as for SC7000 Disk Controllers installed in the VAX-11/750 CPU system (see Appendix A.2).

4.5.3.3 Index and Sector Pulse Signal Selection

This configuration selection is the same as described for SC7000 Disk Controllers in the VAX-11/750 CPU system (see subsection 4.4.2.4).

4.5.3.4 Option Switches

This configuration selection is the same as described for SC7000 Disk Controllers in the VAX-11/750 CPU system (see Appendix A.3).

4.5.3.5 Emulex Bus Terminator

If the V-MASTER/780 assembly is to be installed in the termination slot of the VAX-11/780 CPU chassis, the Emulex Bus Terminator PCBA (Emulex P/N SU7810406) must be installed on the V-MASTER/780 backplane. The Emulex Bus Terminator is electrically identical to the standard DEC Bus Terminator. To install the Bus Terminator PCBA, see Figure 4-10 and use the following procedure:

a. Remove two Phillips-head screws, located to right of bus-out pins and between sections of slot one, as viewed from rear of V-MASTER/780 card cage assembly.

b. Install Bus Terminator PCBA on bus-out pins at left edge of V-MASTER/780 backplane connectors J1 through J6. Verify connectors of Bus Terminator PCBA are fully seated on bus-out pins of backplane.

c. When Bus Terminator PCBA is properly seated on bus-out pins of backplane, replace screws, removed in step a, by inserting them through holes in support bracket for Bus Terminator PCBA. Tighten screws.

d. Connect power supply cables to appropriate jacks on Emulex Bus Terminator PCBA. Jacks have same reference designators as jacks on DEC Bus Terminator PCBA and power supply cables are connected in same way on Emulex Bus Terminator PCBA as on DEC Bus Terminator PCBA (see subsection 4.7).

4.5.3.6 Cable Paddleboard PCBA Installation in V-MASTER

One Cable Paddleboard PCBA is required for each SC7000 Disk Controller. In the VAX-11/780 CPU system, these PCBAs are installed on the backplane of the appropriate slot in the V-MASTER card cage assembly. The procedure assumes the first SC7000 Disk Controller (even TR number if two Controller PCBAs are installed in V-MASTER) is installed in slot three of the V-MASTER with the Cable Paddleboard PCBA installed on the corresponding backplane and that the referenced view is from the rear and toward the backplane.

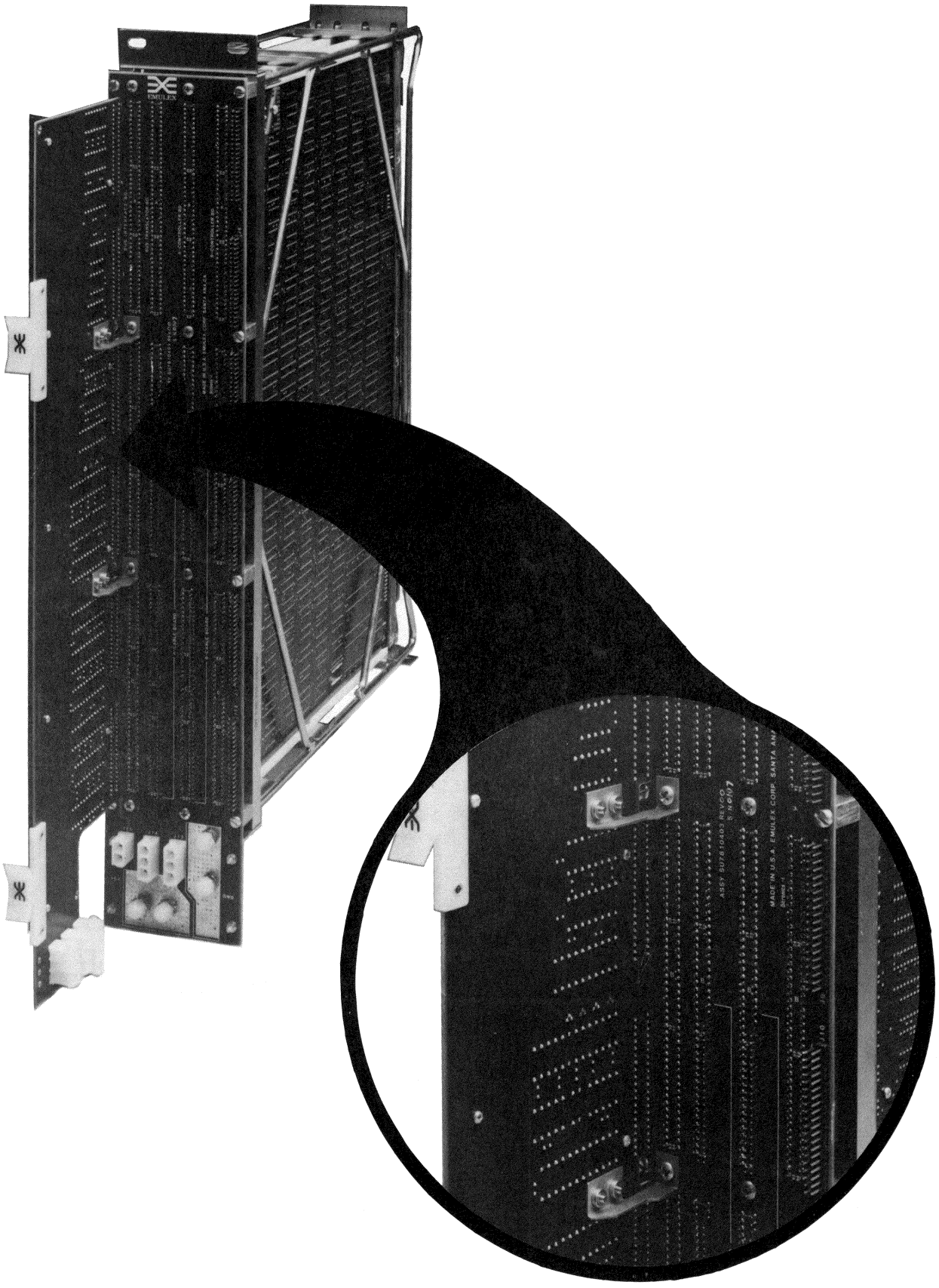


Figure 4-10. Emulex Bus Terminator Installation

An installation kit, Emulex part number TU7813001, is required to install the Cable Paddleboard. To install the Cable Paddleboard PCBA on the V-MASTER/780 backplane, see Figures 4-11 and 4-12, and use the following procedure:

a. Remove Phillips-head screw, located to right side of backplane slot three between sections B and C.

b. Install support bracket on Cable Paddleboard PCBA.

c. Plug A-Cable and all B-Cables into appropriate connectors on Cable Paddleboard PCBA. These six connectors are on left side of PCBA.

d. Do not remove black alignment guides at top of backplane headers.

e. Carefully position three connectors on Cable Paddleboard PCBA over backplane connector pins (sections B and C) of slot three so that white guide on backplane is positioned between connectors on Cable Paddleboard PCBA. When position of PCBA looks and feels as if backplane pins can properly engage connectors on PCBA, gently push PCBA forward until it bottoms on backplane header. When PCBA is properly seated, black alignment guides should be sandwiched between connectors on PCBA and backplane header.

f. Insert screw, removed in step a, through support bracket and tighten in place.

NOTE

Subsequent Cable Paddleboard PCBAs for additional SC7000 Disk Controller are attach to the first Cable Paddleboard PCBA with the standoffs in the installation kit.

4.5.4 SC7000 INSTALLATION IN V-MASTER

The SC7000 Disk Controller may be installed in slot three or four of the V-MASTER/780 card cage assembly. To make installation of the Cable Paddleboard PCBA compatible with the support bracket (see subsection 4.5.3.6, steps a, b, and f), slot three should be used. PCBA installation is the same as steps b, c, and d of subsection 4.4.3.

4.5.5 V-MASTER INSTALLATION IN VAX-11/780 CPU

The V-MASTER/780 card cage assembly may be installed in one of two locations in the VAX-11/780 CPU cabinet, or it may be installed in a DEC or Emulex Expansion cabinet.

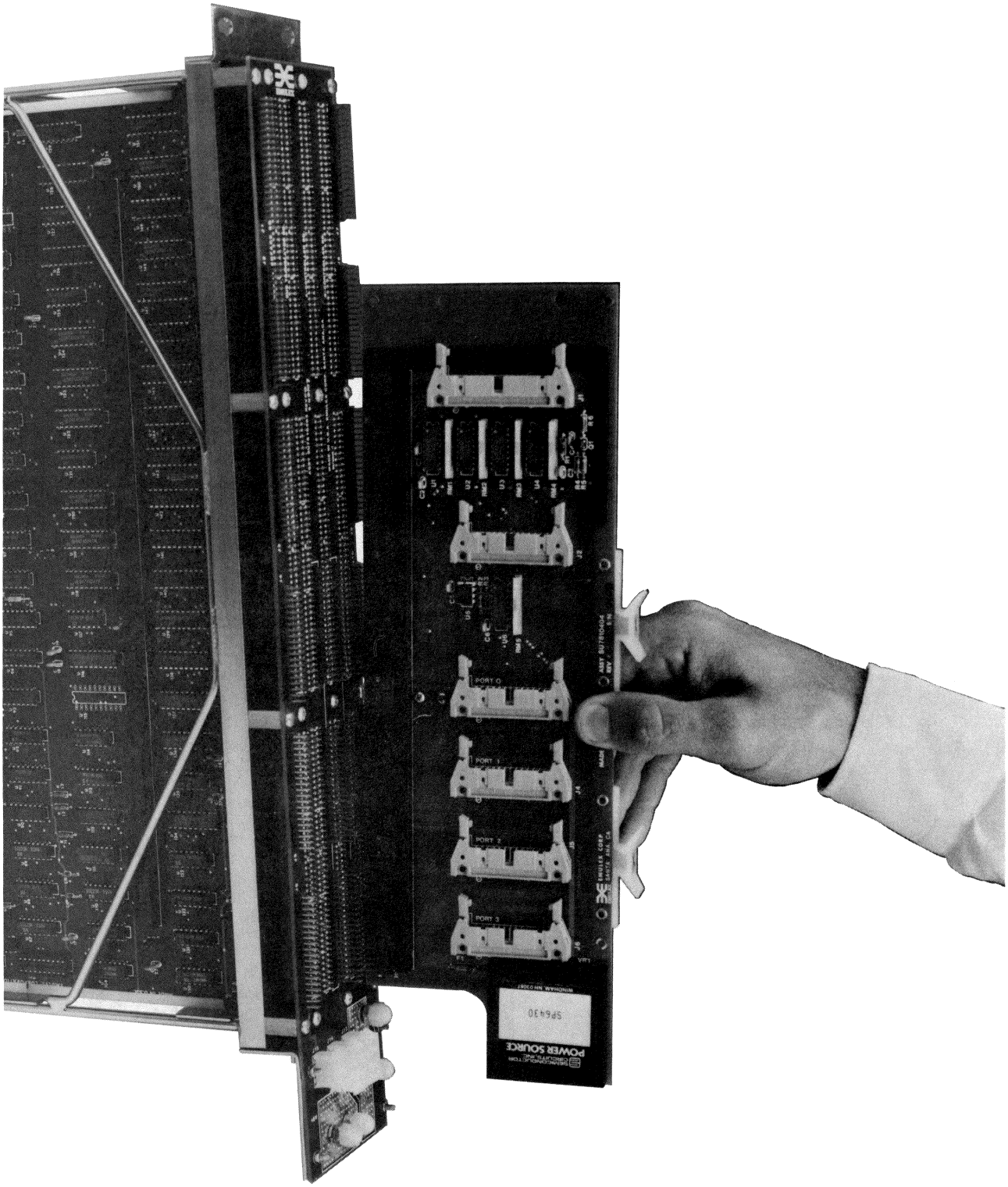


Figure 4-11. Cable Paddleboard PCBA Installation in V-MASTER/780 Card Cage

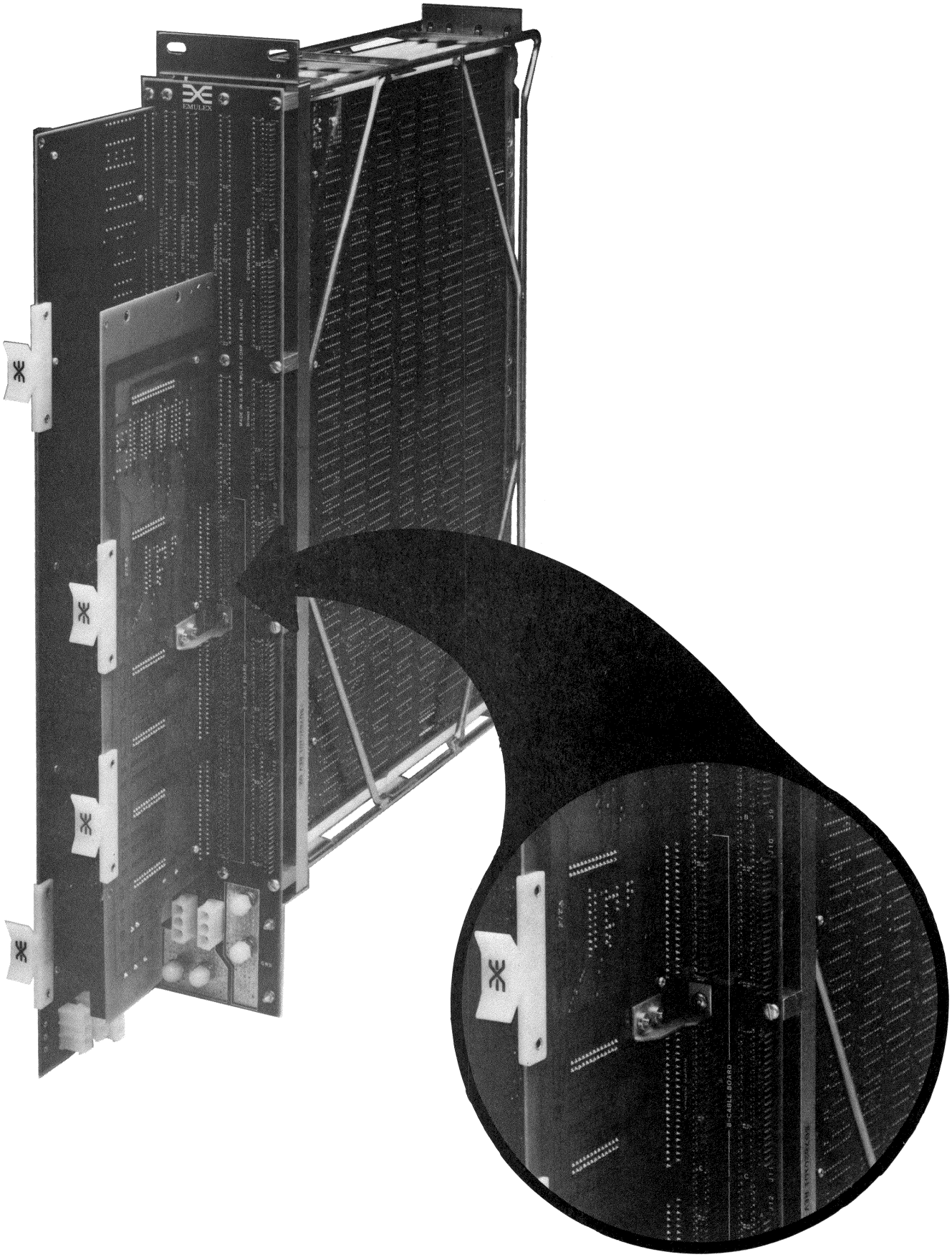


Figure 4-12. Cable Paddleboard PCBA Installation Detail

The most common VAX-11/780 CPU configuration supplied by DEC leaves an empty MBA slot between MBA slot zero and the Bus Terminator PCBA, as shown in Figures 4-13 and 4-14. This empty slot is MBA slot one.

If MBA slot one is not available, the V-MASTER/780 card cage assembly may be installed in the slot occupied by the standard DEC Bus Terminator PCBA. The DEC Bus Terminator PCBA is then replaced by an Emulex Bus Terminator that is installed on the backplane of the V-MASTER/780 card cage assembly (see subsection 4.5.3.6). When this installation method is used, an additional power supply is needed.

If the V-MASTER/780 card cage assembly is to be installed in a DEC Expansion Box cabinet, ask an Emulex Technical Support representative for installation details (see subsection 5.3 for address, etc.).

4.5.5.1 V-MASTER in MBA Slot One

To install the V-MASTER/780 card cage assembly in MBA slot one of the VAX-11/780 CPU cabinet, use the following procedure:

a. Verify CPU power is OFF to avoid injury and/or possible circuit damage.

b. Disconnect coaxial SBI bus cables that link SBI bus and empty DEC MBA card cage chassis.

c. Disconnect all power supply cables from empty DEC MBA card cage chassis, but leave power supply cables connected to power supply.

d. Remove four Phillips-head screws (two upper back and two lower front) that hold empty DEC MBA card cage chassis in place. Save screws.

e. Slide empty DEC MBA card cage chassis backwards out from rear of CPU cabinet.

f. Slide V-MASTER/780 card cage assembly from rear or CPU cabinet forward into MBA slot one position.

g. Secure V-MASTER/780 card cage assembly in place with four Phillips-head screws removed in step d.

h. Connect cables removed in steps b and c to V-MASTER/780 card cage assembly.

4.5.5.2 V-MASTER in Bus Terminator Slot

This installation requires an additional power supply. Two different versions are available from Emulex. Verify the correct version before replacing the dummy power supply with the Emulex

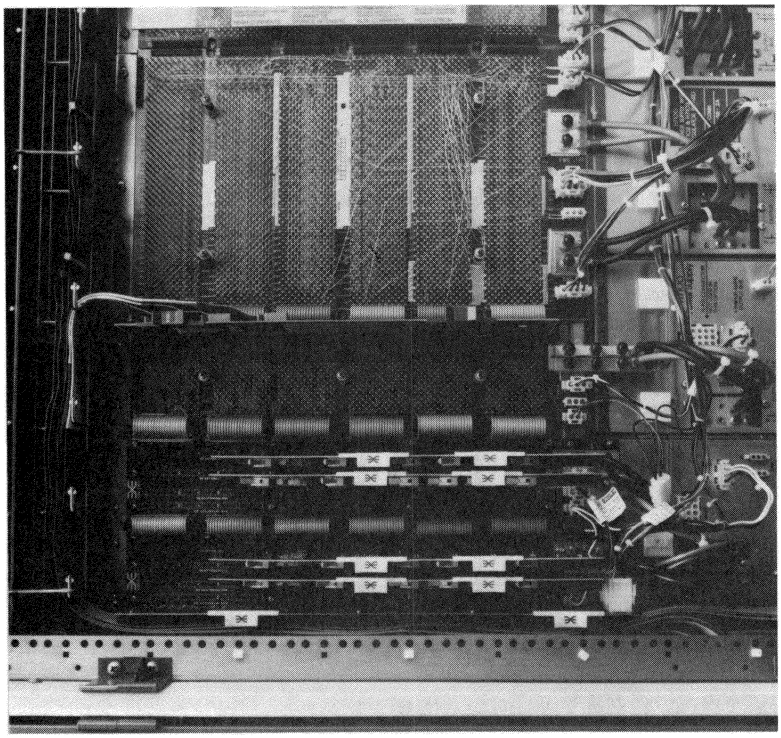


Figure 4-13. Single V-MASTER/780
Card Cage Installation

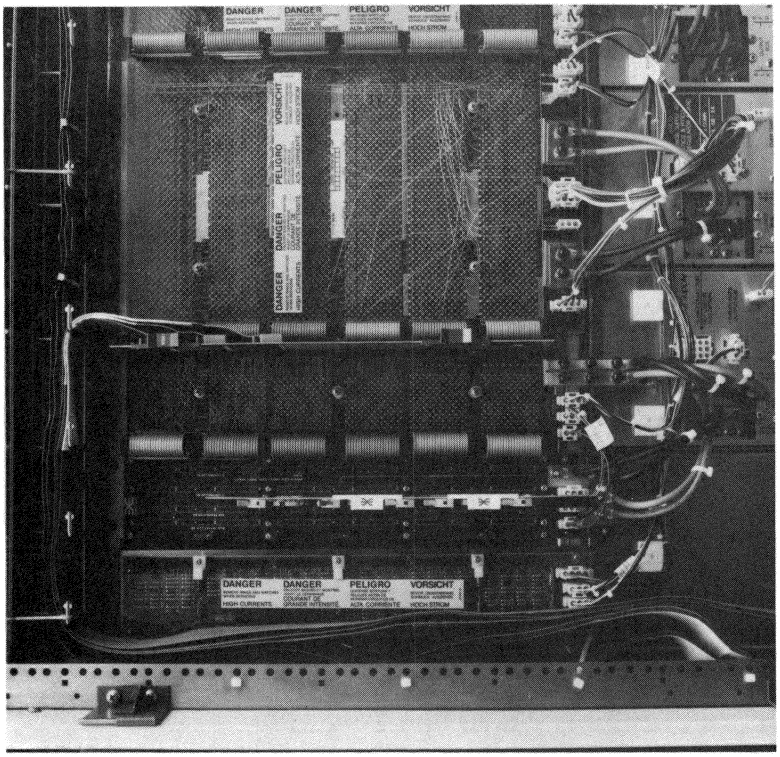


Figure 4-14. Dual V-MASTER/780
Card Cage Installation

power supply. Version -01 is used with a 125 VAC power source and version -02 is used with a 220 VAC power source. The version dash number follows the Emulex part number which is located on the rear side of the power supply near the Emulex logo. Connectors J3 through J7 are also located on the rear side of the power supply.

To install the V-MASTER/780 card cage assembly in the Bus Terminator slot, use the following procedure:

a. Verify CPU power is OFF to avoid injury and/or circuit damage.

b. Disconnect coaxial SBI bus cables that link SBI bus and DEC SBI terminator assembly.

c. Disconnect all power supply cables from DEC SBI terminator assembly but leave power supply cables connected to power supply.

d. Remove four Phillips-head screws (two upper back, two lower front) that hold DEC SBI terminator assembly in place. Save screws.

e. Slide DEC SBI terminator chassis assembly backwards out from CPU cabinet.

f. Install Emulex terminator on loose V-MASTER chassis (see subsection 4.5.3.5).

g. Slide V-MASTER/780 card cage assembly from rear of CPU cabinet forward into MBA slot formerly occupied by DEC SBI terminator.

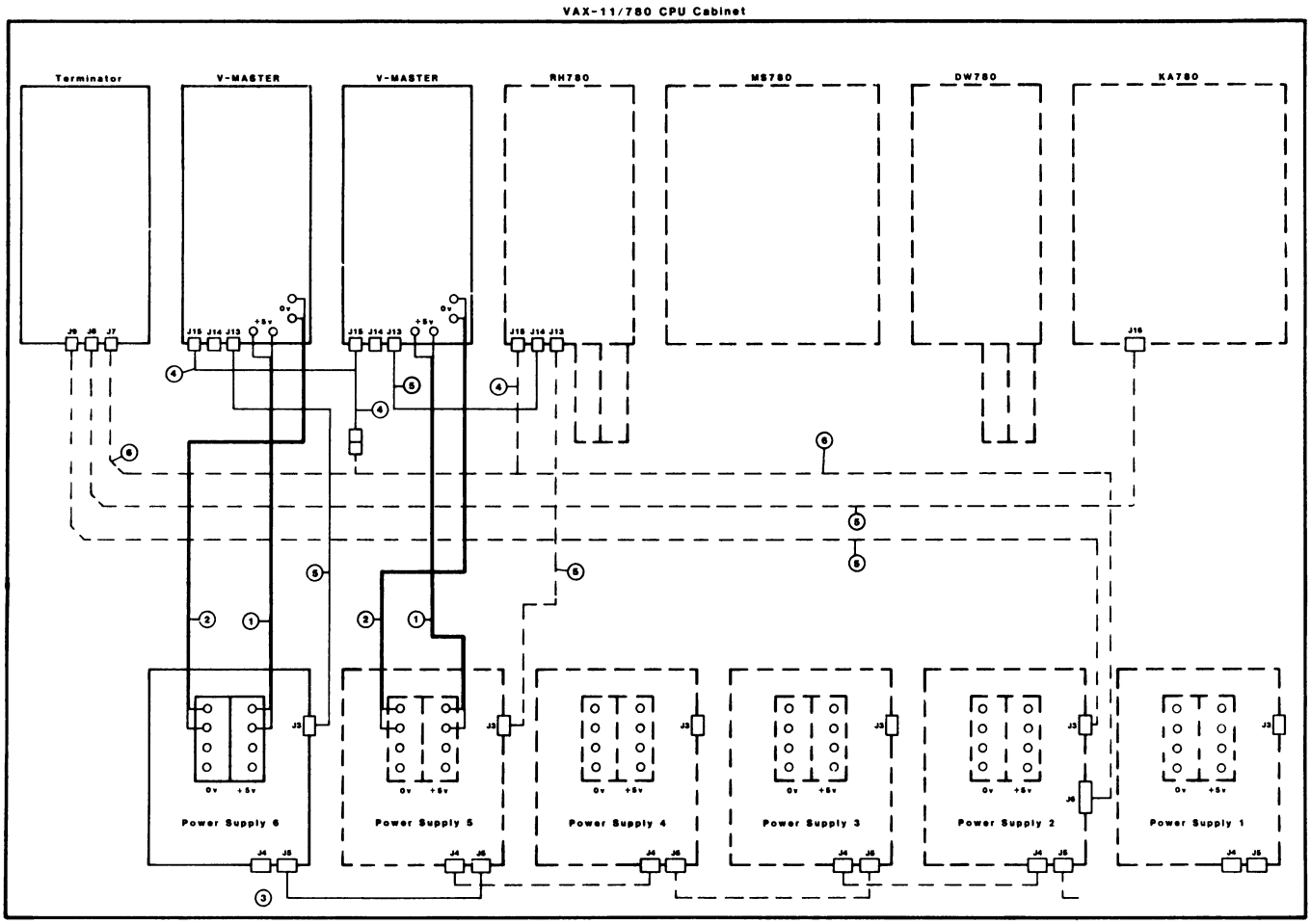
h. Secure V-MASTER/780 card cage assembly in place with four Phillips-head screws removed in step d.

i. Connect SBI bus cable, disconnected in step b, to V-MASTER/780 card cage assembly.

j. Release clasp (rear, center bottom), on dummy power supply located at far left end of CPU cabinet (viewed from rear), by moving clasp toward right side of power supply.

k. Unscrew single Phillips-head screw (front, center top of dummy power supply) and slide dummy power supply out from front of CPU cabinet.

l. Install Emulex power supply in same location from which dummy power supply was removed by reversing steps i and j, then connect power supply cables to V-MASTER/780 card cage assembly. Connections should be made as shown in Figure 4-15.



Legend

No	Description	Color
1	+5vDC	Red
2	0vDC	Black
3	Over Temp	Grey/White
4	-5.2vDC	Blue/Black
5	AC/DC Low	Yellow/Violet/Black
6	-5.2/5 vDC	Red/Black/Blue/Black

— — — DEC Harness and Hardware

——— Emulex Harness and Hardware

Figure 4-15. VAX-11/780 CPU Backplane Cabling Schematic

4.6 BACKPLANE CABLING

The schematic of backplane cabling for VAX-11/780 CPUs is shown in Figure 4-15. The backplane cabling includes +5 Vdc power cables, -5.2 Vdc power cables, AC/DC Low cables, and coaxial SBI bus cables.

4.6.1 +5 VDC POWER CABLES

Each V-MASTER/780 card cage assembly is connected to the appropriate power supply by four cables. These cables are American Wire Gauge (AWG) number eight. Two red cables are for the +5 Vdc side, and two black cables are for the ground side of the power supply. The +5 Vdc cables are run from the +5 Vdc studs on the appropriate V-MASTER/780 backplane to the +5 Vdc terminals on the power supply where they are attached with number 10 machine screws.

The ground cables are run from the ground (GND) studs on the appropriate V-MASTER/780 backplane to the ground terminals on the power supply where they are attached with number 10 machine screws.

NOTE

The number 10 machine screws should already be in place on the power supply; however, spare screws are supplied with the V-MASTER/780 card cage assembly to enable connection if original screws are missing.

4.6.2 -5.2 VDC CABLE

The -5.2 Vdc cable runs from connector J6 on power supply two (second from right as viewed from rear of CPU cabinet) to the connector on the backplane of the CPU, from which a two-wire (blue-wire and black-wire) cable connector is connected to connector J15 on the V-MASTER/780 or to connector J15 on a DEC RH780 MBA. A jumper cable (Emulex P/N SU7811206) is included with the V-MASTER/780 card cage assembly so that a single connector can service two MBA backplane slots.

A combined +5 Vdc/-5.2 Vdc cable terminates at connector J7 of the SBI Bus Terminator PCBA.

4.6.3 AC/DC LOW CABLES

The AC/DC Low cable originates at connector J3 of the power supply for that MBA and terminates at connector J13 on the MBA backplane. If more than one V-MASTER/780 or RH780 is serviced by the power supply, the second unit receives the AC/DC Low signal via a jumper from connector J14 on the first unit to connector J13 on the second unit.

A second set of two AC/DC Low cables form a loop from connector J3 of power supply number two to connector J9 of the SBI Bus Terminator and then returns from connector J8 of the SBI Bus Terminator to connector J16 of the DEC KA780 CPU module backplane.

4.6.4 COAXIAL SBI BUS CABLES

Each chassis in the VAX-11/780 CPU cabinet is linked by six coaxial cables that carry the SBI bus signals. These cables originate at connectors J1 through J6 on the left edge of each chassis and terminate at connectors J7 through J12, respectively, on the right edge of each chassis. The header for each coaxial SBI Bus cable is self-aligning, to ensure no pins are bent when the header is installed, however, the header allows a pair of pins to be open above or below the header, or an entire row of pins to the left or right of the header to be missed. Therefore, after pressing each header into proper position, and before system power up, use a flashlight and carefully inspect each header to verify it is properly installed.

4.7 CABLE ROUTING AND RFI SUPPRESSION

Figure 4-16 is a schematic of disk drive cable routing. Limits for RFI are governed by requirements of the Federal Communications Commission (FCC). This subsection describes the features, use, and installation of the RFI-suppression devices, manufactured by Emulex Corporation, to meet the following FCC requirements:

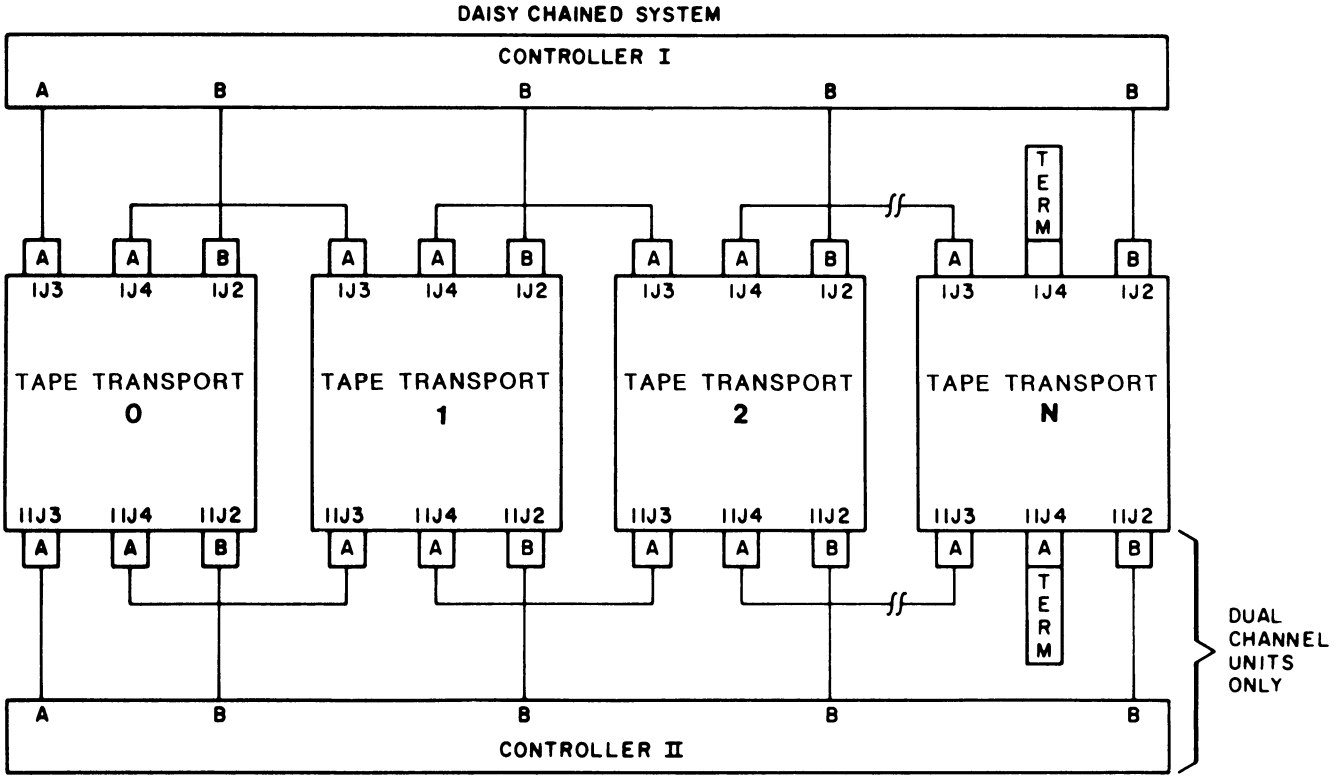
> "This device is a subassembly in the context of Subpart J of Part 15 of FCC Rules. It has been tested in typical packaging and normal usage, and under these conditions, operates within the limitations of Class 'A' equipment.

Excerpt from FCC 83-352 33659 Docket 80-284:

> "Where special accessories, such as shielded cables, are required in order to meet FCC emissions limits, appropriate instructions on the need to use such equipment must be contained in the user manual."

4.7.1 EQUIPMENT CABINET

The equipment cabinet in which the computer equipment is installed should be a standard 19-inch wide EIA or RETMA equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free from holes, except small perforations for air exhaust are permitted.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

Figure 4-16. Disk Drive Cabling Schematic

New equipment cabinets for DEC systems have a specially fabricated rear bulkhead door or panel in which apertures have been cut. These apertures are designed for installation of blank panels or panels with slots and associated grounding bars to provide feed-through shield grounding for cables that connect equipment mounted within the cabinet and equipment mounted in other cabinets. All such apertures must be filled with one of these panels. These panels are called "Personality Panels" and are all the same size, as shown in Figure 4-17.

4.7.1.1 Same Cabinet

If the SC7000 Disk Controller PCBA or V-MASTER/780 card cage assembly with SC7000 Disk Controller PCBA is mounted in the same cabinet as the CPU, the main concern is installing the system so that no gaps are left in the shield. The rear of the CPU cabinet is typically shielded with a bulkhead from top to bottom. The bulkhead is segmented to ease installation of different optional peripheral devices. Each segment has two apertures, each of which is covered by a blank panel. The general procedure is to remove one of the blank panels from the bulkhead segment and replace that blank panel with a Personality Panel (Emulex P/N SU1110201), or to remove the entire bulkhead segment and replace it with a Bulkhead Distribution Panel (Emulex P/N CU2220301). To maintain the integrity of the RFI shield, there must be no gap above or below the replacement panel after that panel is installed. If continuity of shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

4.7.1.2 Separate Cabinets

If the SC7000 Disk Controller PCBA or V-MASTER/780 card cage assembly with SC7000 Disk Controller PCBA is mounted in a separate cabinet from that of the CPU, that expansion cabinet must prevent RFI radiation by being shielded in the same way the DEC CPU cabinet is shielded. Also, the cable that connects to the CMI or VMI in the CPU cabinet must be shielded, since it is external to the shielded cabinet environment.

For installation of related disk drives in separate cabinets, Emulex recommends using a hardened cabinet such as the Everest Electronic Equipment Model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full-length, segmented bulkhead in the rear. One of the segments should be removed and replaced with a Bulkhead Distribution Panel or with a rack-mount panel that contains a blank panel and a Personality Panel (these components are needed to allow the shielded cable from the SC7000 Disk Controller to be terminated). As in the DEC cabinet, there must be no gap above or below any rack-mounted panel when the installation is complete.

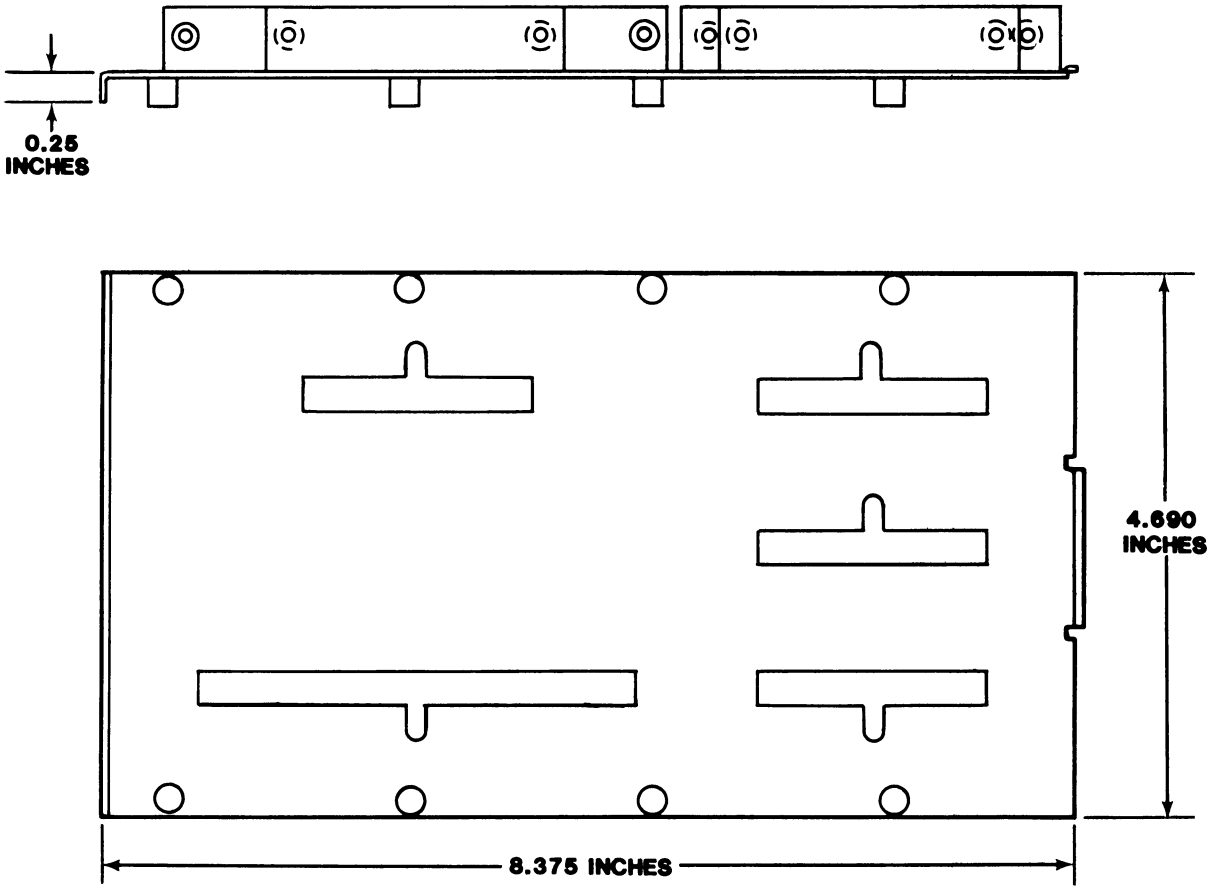


Figure 4-17. Personality Panel Dimensions

To prevent the introduction of conducted interference on the ac line that feeds the internal power supply, a power distribution panel with a line filter must be installed in the expansion cabinet. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated.

4.7.1.3 Shielding

For older equipment-cabinet installations that lack complete metal shielding, all system cabling inside and outside the cabinet must be shielded. For new equipment cabinets that provide complete shielding, only those cables that run outside the cabinet(s) must be shielded.

4.7.1.4 Grounding

Ground returns and shielding of all cabling within the rack/cabinet must be grounded to the cabinet, and the cabinet itself must have a sure Earth ground. All cable ground returns and shielding entering the cabinet must be properly grounded, once inside the cabinet.

NOTE: The procedures below should be followed on any system which mixes Fujitsu Eagle and CDC disk drives on the same daisy chain:

1. Disable Tags 4 and 5 on the Eagle as described on pages 3-7 of the Fusjitsu manual.

2. Use one of the following three grounding procedures:

A. Install CDC drives with chassis (AC) and signal (DC) grounds connected together at the drive. Refer to the system grounding section of the CDC drive manual for details.

Install grounding strap SG (DC) to FG1 (AC) on the Eagle.

Install separate ground straps from each drive to the common system ground on the CPU.

B. Install FCC-approved drive cables and attach all cable shields to the CPU and drive chassis grounds.

C. Separate the chassis (AC) and signal (DC) grounds on each drive.

Install FCC-approved cables and attach the shield grounds to the chassis (AC) ground of each drive. Daisy chain the

signal (DC) ground of each drive to the signal (DC) ground of the controller.

3. If the cable from the controller to the **first** drive is less than 25 feet, place the Eagles first in the daisy chain. If the cable from the controller to the **first** drive is more than 25 feet, place the Eagles last on the daisy chain, closest to the terminator. If the **total** daisy chain length is more than 50 feet, use FCC approved cables whenever possible.

4.7.2 RFI-SUPPRESSION DEVICES

The RFI-suppression devices developed by Emulex consists of suitable Personality Panels, unshielded cables for connections within the equipment cabinet, and shielded/jacketed cables that are routed between the cabinets. Two Personality Panels are required for each shielded cable; one for each end of the shielded/jacketed cable(s). The Personality Panel for the disk controllers is Emulex part number (P/N) SU1110201.

For older equipment cabinets that lack the bulkhead with apertures for blank panels and Personality Panels, Emulex provides a special bulkhead panel (Emulex P/N CU2220301) that can be mounted on the back of an equipment cabinet. Mounting requires two screws on each end, as shown in Figure 4-18. This distribution panel has apertures for the blank panels and Personality Panels.

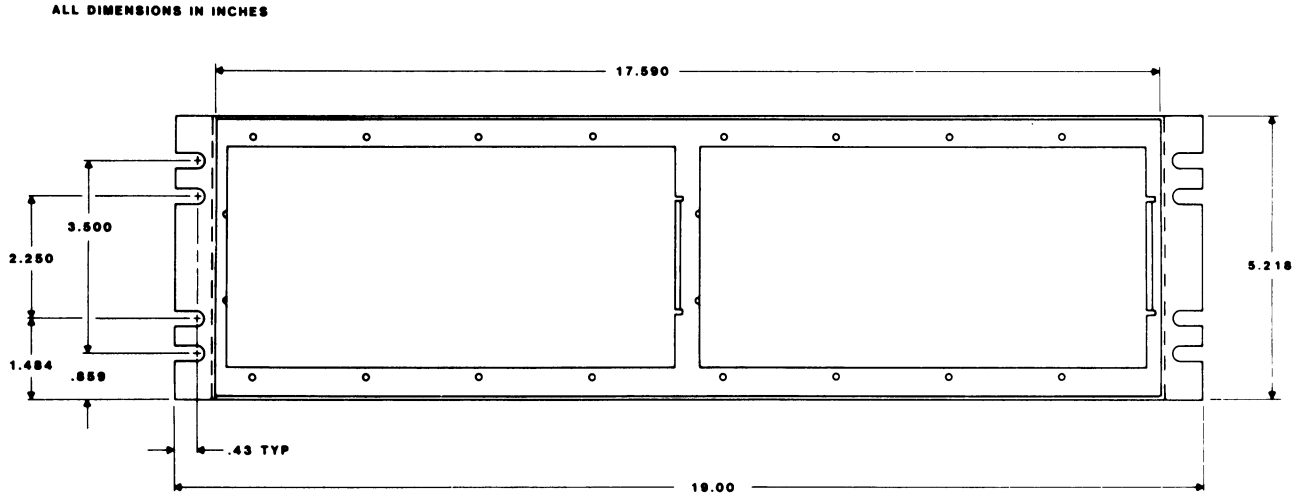


Figure 4-18. CU2220301 Bulkhead Panel

Cable details for the disk controllers are listed in Table 4-11 with cable lengths expressed in feet (ft) or inches (in.), as applicable.

Table 4-11. Shielded Cables and Installation Hardware

Item	Part Number	Description	Qty Rqd	Interface
1	SU7811212-01	Cable, Shielded, 4 ft	1	SMD A-Cable
	SU7811212-02	Cable, Shielded, 8 ft	1	SMD A-Cable
	SU7811212-03	Cable, Shielded, 15 ft	1	SMD A-Cable
	SU7811212-04	Cable, Shielded, 25 ft	1	SMD A-Cable
	SU7811212-05	Cable, Shielded, 35 ft	1	SMD A-Cable
	SU7811212-06	Cable, Shielded, 50 ft	1	SMD A-Cable
2	SU7811215-01	Cable, Unshielded, 2 ft	1	SMD A-Cable
	SU7811215-02	Cable, Unshielded, 4 ft	1	SMD A-Cable
	SU7811215-03	Cable, Unshielded, 6 ft	1	SMD A-Cable
	SU7811215-04	Cable, Unshielded, 8 ft	1	SMD A-Cable
	SU7811215-05	Cable, Unshielded, 10 ft	1	SMD A-Cable
	SU7811215-06	Cable, Unshielded, 12 ft	1	SMD A-Cable
	SU7811215-07	Cable, Unshielded, 15 ft	1	SMD A-Cable
3	SU7811219-01	Cable, Unshielded, 2 ft	2	SMD A-Cable
	SU7811219-02	Cable, Unshielded, 4 ft	2	SMD A-Cable
	SU7811219-03	Cable, Unshielded, 6 ft	2	SMD A-Cable
	SU7811219-04	Cable, Unshielded, 8 ft	2	SMD A-Cable
	SU7811219-05	Cable, Unshielded, 10 ft	2	SMD A-Cable
4	SU7811213-01	Cable, Shielded, 4 ft	1-4	SMD B-Cable
	SU7811213-02	Cable, Shielded, 8 ft	1-4	SMD B-Cable
	SU7811213-03	Cable, Shielded, 15 ft	1-4	SMD B-Cable
	SU7811213-04	Cable, Shielded, 25 ft	1-4	SMD B-Cable
	SU7811213-05	Cable, Shielded, 35 ft	1-4	SMD B-Cable
	SU7811213-06	Cable, Shielded, 50 ft	1-4	SMD B-Cable
5	SU7811218-01	Cable, Unshielded, 2 ft	2-8	SMD B-Cable
	SU7811218-02	Cable, Unshielded, 4 ft	2-8	SMD B-Cable
	SU7811218-03	Cable, Unshielded, 6 ft	2-8	SMD B-Cable
	SU7811218-04	Cable, Unshielded, 8 ft	2-8	SMD B-Cable
	SU7811218-05	Cable, Unshielded, 10 ft	2-8	SMD B-Cable
	SU7811218-06	Cable, Unshielded, 12 ft	2-8	SMD B-Cable
	SU7811218-06	Cable, Unshielded, 15 ft	2-8	SMD B-Cable
6	SU1110201	Personality Panel	4-10	All
7	CU2220301	Bulkhead Distribution Panel (optional)	2-5	All

The items listed in Table 4-11 can be ordered from your Emulex sales representative or directly from the factory. The factory address is:

Emulex Customer Service
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

4.7.3 CABLE INSTALLATION

Most Emulex products are installed directly in the CPU system cabinet manufactured by DEC. The peripheral(s) controlled by the Emulex products are usually housed in separate equipment cabinets, and the cabinets provide the shielding for the equipment, but cabling between equipment and external to the cabinet(s) must be shielded and all shielding must be grounded. If the cabinets are older types which do not provide complete shielding, all interconnecting cables must be shielded and properly grounded even when not routed outside cabinets.

When peripherals controlled by the Emulex product(s) are not housed in the same equipment cabinet, the equipment must be interconnected by suitable RFI-suppression devices that ground all shielded cables entering the equipment cabinet.

To install the Emulex RFI-suppression devices, see Figures 4-17 and 4-19 and use the following procedure:

a. Open rear bulkhead door or panel of CPU equipment cabinet.

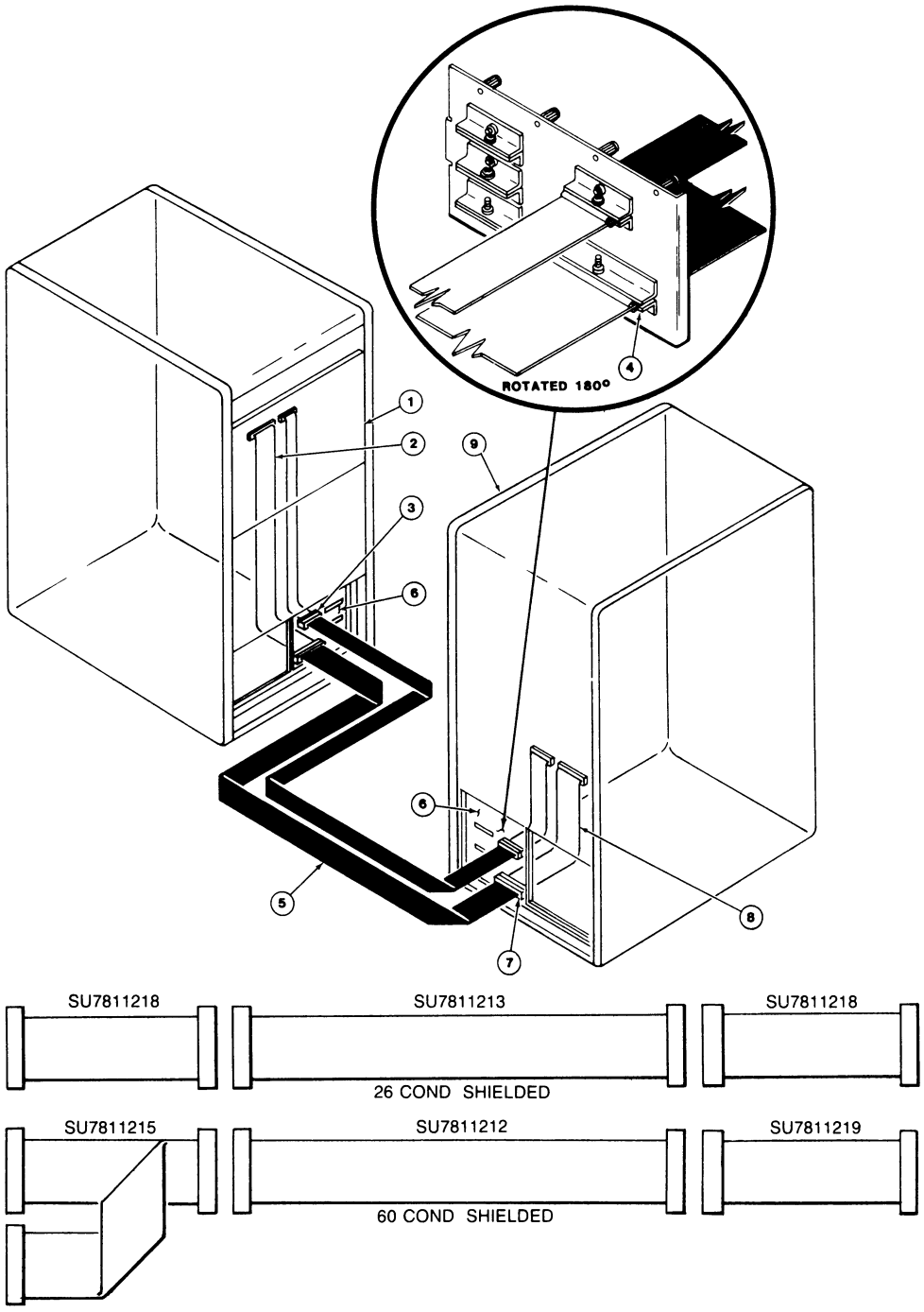
b. Install Emulex SC7000 Disk Controller or V-MASTER/780 card cage in appropriate CPU bus slots (see subsection 4.4.3 or 4.5.5, as applicable).

c. Install appropriate Personality Panel in convenient aperture in rear bulkhead of equipment cabinet for SC7000 Disk Controller and secure in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panel.

d. Install two Personality Panels in convenient aperture in rear bulkhead of equipment cabinet for first disk drive in daisy chain and secure each in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panels.

e. Repeat step d for cable entry to and exit from cabinets for remaining disk drives to be in daisy chain.

f. Select shielded interface cable (P/N SU7811212) long enough to reach from Personality Panel for SC7000 Disk Controller to Personality Panel for cable entry to first disk drive.



1. SC7000 DISK CONTROLLER PCBA
2. NONSHIELDED EXTENSION CABLE, SC7000 DISK CONTROLLER - SHIELDED CABLE
3. CABLE CONNECTORS, SC7000 DISK CONTROLLER - SHIELDED CABLE
4. CLAMP - SHIELD OF SHIELDED CABLE CLAMPED WITHIN
5. SHIELDED/JACKETED CABLE, EXTERNAL TO EQUIPMENT CABINETS
6. PERSONALITY PANELS
7. CABLE CONNECTORS, SHIELDED CABLE - PERIPHERAL DEVICE
8. NONSHIELDED EXTENSION CABLE, SHIELDED CABLE-PERIPHERAL DEVICE
9. PERIPHERAL DEVICE OR V-MASTER/780

Figure 4-19. RFI-Suppression Cable Installation

g. Strip about one inch of shielded insulation from end of cable for SC7000 Disk Controller to expose shield. Cut shield at each edge to allow shield to be folded back over insulation, then fold shield over insulation. Route prepared cable ends through appropriate slots in Personality Panel (see detail in Figure 4-19). Repeat this process at other end of cable.

h. Select unshielded interface cable (P/N SU7811215) long enough to reach from A-Cable connector on SC7000 Disk Controller to associated Personality Panel in cabinet bulkhead.

i. Find arrow molded into header of cable connector for mating cable connector. Arrow identifies pin 1 of connector.

j. Find arrow molded into header of mating connector on SC7000 Disk Controller, then align arrows and connect mating connectors.

k. Repeat steps h through j with unshielded interface cable (P/N SU7811219) at disk drive end of shielded A-Cable.

l. Select shielded interface cable (P/N SU7811213) long enough to reach from Personality Panel for SC7000 Disk Controller to Personality Panel for first disk drive in daisy chain.

m. Repeat steps g through j for this B-Cable, then repeat this B-Cable installation procedure for up to three more B-Cables.

n. Select unshielded interface cable (P/N SU7811218) long enough to reach from B-Cable connector on SC7000 Disk Controller to shielded B-Cable connector in associated Personality Panel for SC7000 Disk Controller.

o. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.

p. Select unshielded interface cable (P/N SU7811219) long enough to reach from B-Cable connector on disk drive to associated Personality Panel in rear bulkhead of disk drive cabinet.

q. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.

r. Repeat steps n through q for each of remaining B-Cables.

s. Interconnect disk drives to be daisy chained as instructed in disk drive technical manual. Verify last disk drive in daisy chain is properly terminated. If disk drives are in separate extension cabinets, use shielded cable between cabinets as described in foregoing steps of this procedure.

t. Close bulkhead door or panel on each equipment cabinet.

The subsystem cabling for the SC7000 Disk Controller and associated disk drives is shown in Figure 4-16. B-Cables are radially connected, one to each disk drive, but the A-Cable is connected to only the first disk drive and thence to subsequent disk drives in the daisy chain by additional A-Cables between disk drives.

4.7.4 A-CABLE INSTALLATION

The 34-pin flat-cable connector J1 and the 26-pin flat-cable connector J2 at the top of the Cable Paddleboard PCBA are used for the A-Cable which can be daisy chained to all the disk drives for control and status signals. Two connectors are used for the 60-conductor A-Cable to reduce the size of the PCBA; therefore, the interface does require a specially split A-Cable. Pin 1 on each connector is located on the left side of the connector when viewed from the component side of the PCBA. The circuitry on the Cable Paddleboard PCBA provides the A-Cable drivers.

In addition to FCC requirements, other A-Cable installation details must be done before the system can function properly. The end of the 60-wire A-Cable that mates with the A-Cable connectors on the Cable Paddleboard PCBA is split so that 34 wires go to one A-Cable connector and 26 wires go to the other A-Cable connector. A triangle-shaped arrowhead is molded into the body of each connector plug and jack. The arrowhead points to pin one on the left side of the connector. The arrowheads of mating connectors must be aligned so pin one of the plug is connected to pin one of the jack.

NOTE

Cable connectors for flat cables are not keyed and can be physically reversed. No damage should result from the cable reversal, but the system cannot operate.

If more than one physical disk drive is to be installed in the system, the A-Cable is daisy-chained from the first disk drive to the other disk drive by the one-to-one daisy-chain A-Cable. The last disk drive on the daisy-chained A-Cable must have a terminator installed. The terminator is supplied by the disk drive manufacturer, and is usually plugged into one of the two A-Cable connectors on the disk drive. In some disk drive models, a ground wire emerges from the terminator assembly. This ground wire must be connected to the chassis of the disk drive to provide a ground return for the resistors in the terminator assembly.

4.7.5 B-CABLE INSTALLATION

The four 26-pin flat-cable connectors J3, J4, J5, and J6 on the Cable Paddleboard PCBA are for the radial B-Cables which are used to connect four physical disk drives to the SC7000 Disk Controller. Pin 1 of each connector is located on the left side of the connector when viewed from the component side of the PCBA. The four B-Cable ports are all identical and any disk drive may be plugged into any B-Cable connector.

Each physical disk drive is radially connected to the Cable Paddleboard PCBA by an individual B-Cable (see Figure 4-16). It makes no difference which B-Cable port on the Cable Paddleboard PCBA is used by which disk drive. No external terminators are used with the B-Cable. Pin matching follows the same rules as described for the A-Cable (see subsection 4.7.4).

4.7.6 GROUND STRAP

For proper operation of the disk drive subsystem, the physical disk drives **must** have a sure ground connection to the chassis ground of the computer. This ground connection should be made with metal braid at least 1/4-inch wide (preferably insulated) or with AWG number 10 wire or larger. The grounding strap or wire may be daisy chained between the disk drives.

NOTE

Failure to observe proper grounding methods can result in marginal operation with random-error conditions.

4.8 TESTING

Testing is performed by the Self-Test routine in the SC7000 Disk Controller and by running separate diagnostic programs. This subsection describes tests, register examination procedures and hardware formatting of the disks. Except for the Self-Test routine, the procedures for VAX-11/750 CPU systems differ slightly from the procedures for VAX-11/780 CPU systems.

4.8.1 SELF-TEST ROUTINE

When power is applied to the CPU, the SC7000 Disk Controller automatically executes a built-in Self-Test routine. This Self-Test routine is not executed with every programmed I/O INIT condition, but only when the CPU is powered up. If the Self-Test routine is executed successfully, the FAULT light emitting diode (LED) on the front edge of the SC7000 Disk Controller PCBA is not lit. A steadily lit FAULT LED indicates the SC7000 Disk Controller failed the Self-Test routine and cannot be addressed from the CPU. A flashing FAULT LED indicates the SC7000 Disk Controller Self-Test routine was successful but no disk drive is connected, or if

connected, the disk drive is not in the Power-On state. A slowly flashing FAULT LED indicates two disk drives have the same address.

4.8.2 REGISTER EXAMINATION

Before formatting the disk(s) or running diagnostics, a quick check should be made to verify the controller registers can be read from the CPU console.

4.8.2.1 With VAX-11/750 CPU

To verify controller registers can be read from the VAX-11/750 CPU console, use the following procedure:

a. Power up CPU with POWER ON ACTION/HALT switch in HALT position.

b. When CPU has completed its Self-Test routine, a >>> prompt symbol should be issued at the console to indicate console is in I/O mode. Check FAULT indicator on SC7000 Disk Controller; if not steadily lit, examine contents of first MBA register on SC7000 Disk Controller. For RH0, this examination is done by typing:

```
>>> E    F28004<cr>
```

c. Use Base Address F2A004 for RH1.

d. Use Base Address F2C004 for RH2.

e. If SC7000 Disk Controller cannot be accessed at Base Address, console should return:

```
"?"
```

otherwise, console should return:

```
00000000
```

which is current contents of first MBA register.

f. Verify address and data path by testing MBA Byte Count Register (Base Address + 10) as described in subsection 4.8.2.2.

4.8.2.2 With VAX-11/780 CPU

To verify controller registers can be read from the VAX-11/780 CPU console, use the following procedure:

a. Power-up CPU.

b. When CPU has loaded WCS from its (floppy) disk drive, LOAD DONE should be printed at the console, followed by a >>> prompt symbol to indicate console is in I/O mode. Check FAULT LED indicator on SC7000 Disk Controller; if not steadily lit, examine contents of first MBA register on SC7000 Disk Controller. For TR10, this examination is done by typing:

```
>>> E   20014000<cr>
```

c. Use 20012000 for TR9.

d. Use 20016000 for TR11.

e. If SC7000 Disk Controller cannot be accessed at Base Address, console should return an invalid response, otherwise, it should return 00000020, which is current contents of first MBA register.

The data path between the SBI and the SC7000 Disk Controller can be verified by loading a word (four hexadecimal digits) into the MBA Byte Count Register (Base Address + 10). When the contents of this register are examined, the firmware should have copied into the upper half of this longword register the word that had been deposited into the lower half of this longword register. Various combinations of four hexadecimal digits should be exercised to ensure the data is deposited correctly.

If the SC7000 Disk Controller fails any of the Self-Test routine or register deposit/examine operations, see Appendix E.

4.8.3 HARDWARE FORMATTING THE DISK

The SC7000 Disk Controller can format the disk by writing headers and zero data bits in all sectors of the disk. This format does not verify the data or headers, nor does it write a Bad Sector File on the last track of the last cylinder.

The CPU console should already be in the I/O mode (indicated by >>> prompt symbol). If the CPU console is not in the I/O mode, type CNTL P to place CPU console in I/O mode.

4.8.3.1 Formatting with VAX-11/750 or VAX-11/780 CPU

The Base Address for the first disk drive on RH0 is F28400, on RH1 it is F2A400, and on RH2 it is F2C400. For each disk drive after the first disk drive add 80 to the previous Base Address.

The Base Address for the first disk drive on TR8 is 20010400, on TR9 it is 20012400, and on TR10 it is 20014400. For each disk drive after the first disk drive add 80 to the present Base Address.

If the disk drive is in the On-Line mode with no disk drive errors, format the disk drive by using the following procedure:

NOTE

The addresses in this formatting example are for logical disk drive unit zero on TR10. A <cr> indicates a carriage return, and spaces should be placed as indicated.

a. Deposit 0001 in MBACR (MBA Base Address +04) to initialize V-MASTER/780:

>>> D/L/P (Base Address + 04) 0001<cr>

b. Deposit 0013 (Pack Acknowledge command) in RMCS1 (disk drive Base Address):

>>> D/L/P (Base Address + 400) 0013<cr>

c. Examine contents of RMDS (disk drive Base Address +04) to check disk drive status:

>>> E/L/P (Base Address + 404)<cr>

Console should return printout:

P (Base Address + 404) 000011C0

This response indicates medium is on line, disk drive is present and ready, and volume is valid.

d. Deposit FFFF (enables optional Format command) in RMHR (disk drive Base Address +42C):

>>> D/L/P (Base Address + 42C) FFFF<cr>

e. Deposit 003F (Format command) in RMCS1 (disk drive Base Address):

>>> D/L/P (Base Address + 400) 003F<cr>

ACTIVITY LED indicator should flash as long as formatting is in process.

f. When ACTIVITY LED indicator stops flashing, examine contents of RMDS (disk drive Base Address + 04) to determine if ERR (bit 14) is set to indicate an Error status condition:

>>> E/L/P (Base Address + 404)<cr>

If no Error status is present, RMDS should contain 15C0. If there is an error, as a result of Format operation, contents of RMER1 and RMER2 should be examined to determine cause of error, and contents of RMDA and RMDC

should be examined to determine how far formatting progressed.

Time required to format a standard-size disk depends on the emulation:

RM03 needs 1.8 minutes
RM05 needs 5.5 minutes
RM80 needs 4.5 minutes.

4.8.4 DEC DIAGNOSTICS

The SC7000 Disk Controller can execute the DEC disk diagnostic programs, defined in this subsection, if the disk drive has standard RM03, RM05, or RM80 capacity. For more detailed information about these DEC disk diagnostic programs, see Appendix C.

4.8.4.1 Diagnostic for VAX-11/750 CPU System

The VAX-11/750 CPU/disk drive system is tested by the DEC diagnostic programs in the following list:

ECCAA - VAX-11/750 RM750 Diagnostic

This program tests only the RH750 portion of the SC7000 Disk Controller. Most of the test is executed with the SC7000 Disk Controller in the Diagnostic mode which allows simulation of an attached Massbus. Since the SC7000 Disk Controller has no Massbus, it does not simulate a Massbus; therefore, only Tests 1, 2, 3, 5, and 6 run without errors.

4.8.4.2 Diagnostic for VAX-11/780 CPU System

The VAX-11/780 CPU/V-MASTER/disk drive system is tested by the DEC diagnostic programs in the following list:

ESCAA - VAX-11/780 RH780 Diagnostic

This program tests only the RH780 portion of the SC7000 Disk Controller. Most of the test is executed with the SC7000 Disk Controller in the Diagnostic mode which allows simulation of an attached Massbus. Since the SC7000 Disk Controller has no Massbus, it does not simulate a Massbus; therefore, only Tests 1, 2, 3, 5, and 6 run without errors.

4.8.4.3 Diagnostics Common to VAX-11/750 and VAX11/780 CPU Systems

EVRDA - RM03/RM05/RM80 Diskless Diagnostic

This program tests the disk drive portion of the logic in the SC7000 Disk Controller. No Data Transfer operations are performed. Part of this program uses the Diagnostic mode of the DEC disk drives. Since this Diagnostic mode is not implemented in the SC7000 Disk Controller, only Tests 1 through 23 run without errors.

EVRAC - Disk Formatter

This program formats RM03 and RM05 types of disk drives. A different Format program is used for RM80 types of disk drives.

EVRDB - RM03/RM05 Functional

This program does simple operations, including Data Transfer operations, with an attached RM03 or RM05 disk drive.

EVRGA - RM80 Formatter

This program formats RM80 types of disk drives.

EVRGB - RM80 Functional Diagnostic

This program does simple operations, including Data Transfer operations, with attached RM80 types of disk drives.

EVRAA - VAX RP/RK/RM/RX/TU58 Reliability

This program is a general-purpose data reliability test program which handles RM types of disk drives.

NOTE

Corresponding Emulex diagnostics that relate to VAX systems are contained in separate manuals and may be ordered from Emulex.

Section 5
TROUBLESHOOTING

5.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the SC7000 Disk Controller system. This section is divided into five subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	Preventive Maintenance
5.3	Service
5.4	General Fault Isolation Procedures
5.5	Specific Fault Isolation Procedures

5.2 PREVENTIVE MAINTENANCE

The regularly scheduled maintenance checks, cleaning procedures, component replacement procedures and adjustment procedures detailed in the separately supplied system component technical manuals should be accomplished at the prescribed intervals. There are no adjustments or calibrations required in servicing the SC7000 Disk Controller system. Emulex recommends the diagnostic software programs be used in the system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circuit component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

Preventive maintenance of the SC7000 Disk Controller system also includes three periodic verifications:

a. Proper seating of the SC7000 Disk Controller PCBAs in CPU backplane or V-MASTER/780 card cage assembly.

b. Proper seating and mating of cables in connectors.

c. Proper seating of PROMs in their respective IC sockets.

These verifications should be made about once a year or whenever physical location or component of the SC7000 Disk Controller system is changed.

5.3 SERVICE

The components of the Emulex SC7000 Disk Controller system have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory. Corrective maintenance should not normally be required. Except for setting DIP switches and placing jumpers on proper connective points (see subsection 4.5), no adjustments or alignments are required. If a malfunction does occur, as indicated by Fault Isolation procedures, and a component is not working properly, the entire SC7000 Disk Controller should be returned to the factory or to an Emulex-authorized repair center for service.

5.3.1 EXPEDITING

If the SC7000 Disk Controller is to be returned, Emulex recommends that a description of the symptoms and operating environment be included with the returned unit to expedite troubleshooting. Figure 5-1 shows a configuration record sheet to be filled in. The depicted configuration shows component locations, PROMs, DIP switch settings and cable connections.

Before returning the SC7000 Disk Controller to Emulex, whether it is or is not under warranty, request the factory or the factory representative to provide return-shipment instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A PRODUCT OR COMPONENT TO EMULEX
WITHOUT AUTHORIZATION

A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii notify:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

Outside of the United States, notify the distributor from whom the product or component was initially purchased.

After notifying Emulex and receiving an RMA, package the product (preferably by using the original packing material) and send the product **POSTAGE PAID** to the address provided by the Emulex representative. The sender must also insure the package.

1. Emulation PROM range from _____ to _____

2. Switch settings (circle 1 or 0)

SW1

1	2	3	4	5	6
0	0	0	0	0	0
1	1	1	1	1	1

SW2

1	2	3	4	5	6
0	0	0	0	0	0
1	1	1	1	1	1

SW3

1	2	3	4	5	6
0	0	0	0	0	0
1	1	1	1	1	1

SW4

1	2	3	4	5	6
0	0	0	0	0	0
1	1	1	1	1	1

SW5

1	2	3	4
0	0	0	0
1	1	1	1

SW6

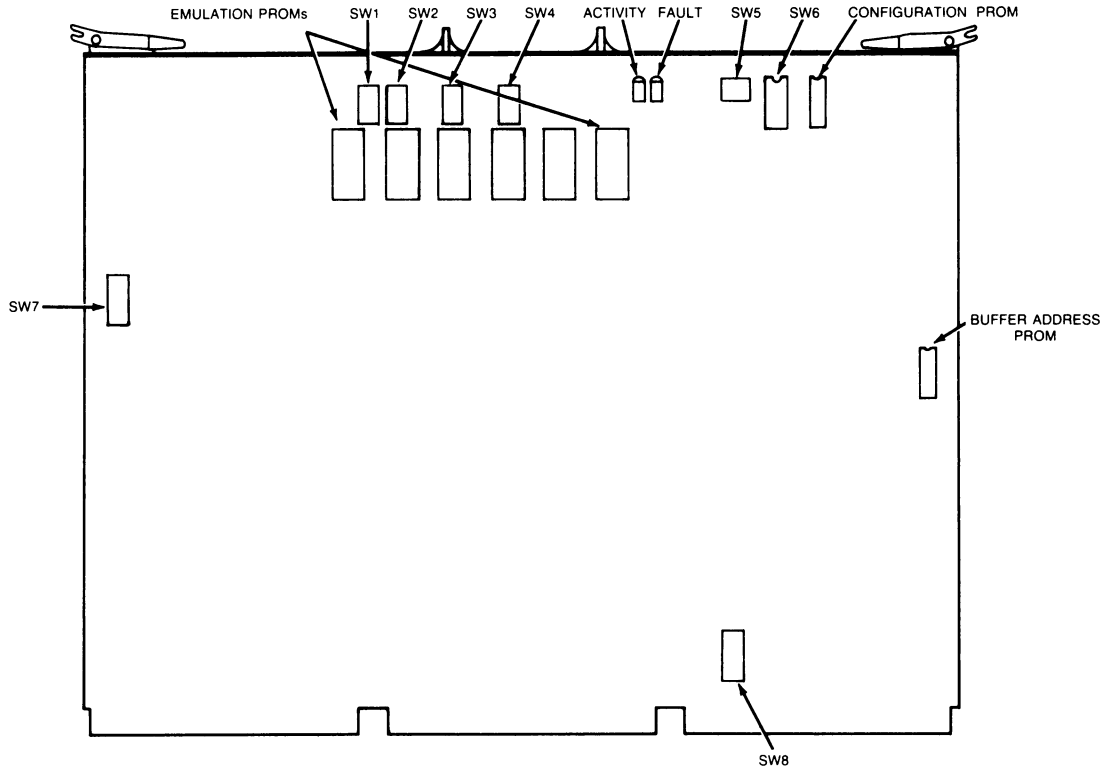
1	2	3	4
0	0	0	0
1	1	1	1

SW7

1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1

SW8

1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1

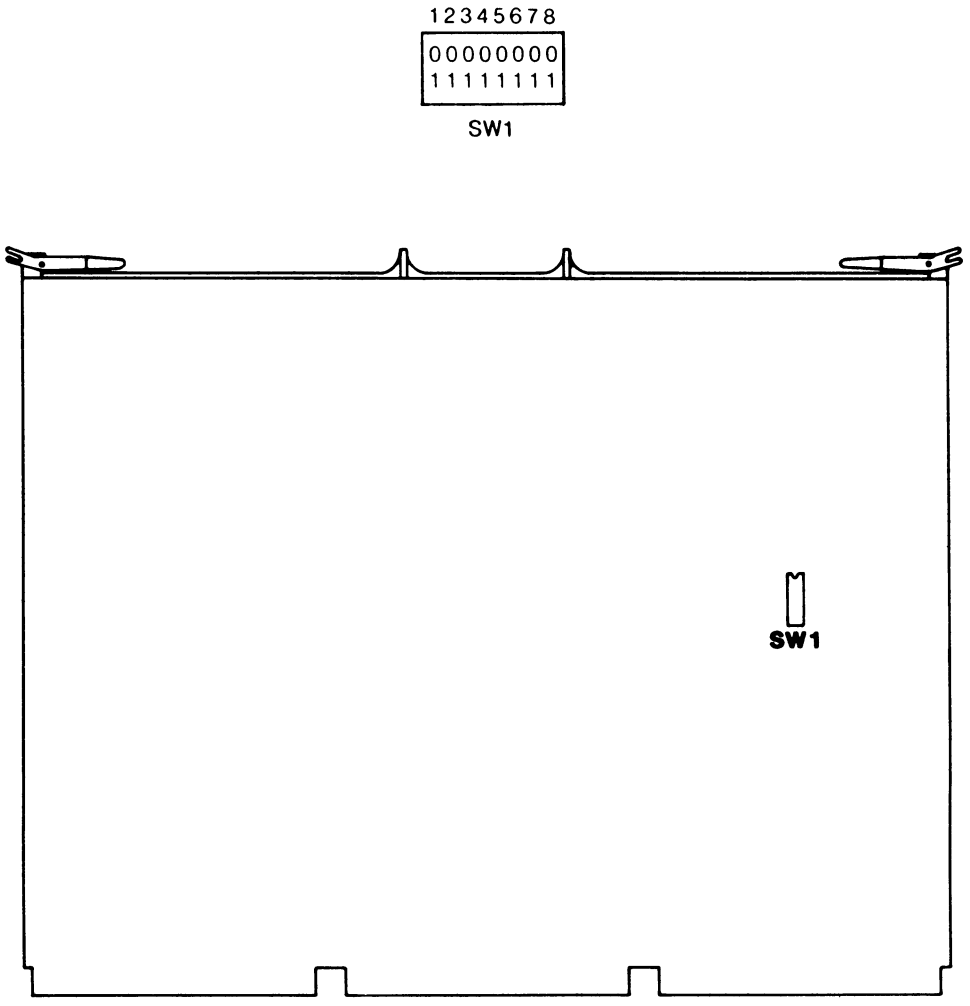


Disk Controller PCBA

Use Pencil

Figure 5-1. Configuration Record Sheet (SH 1 of 3)

1. Emulation PROM numbers range from _____ to _____
2. Switch settings (circle 1 or 0)



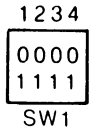
Bus Interface PCBA

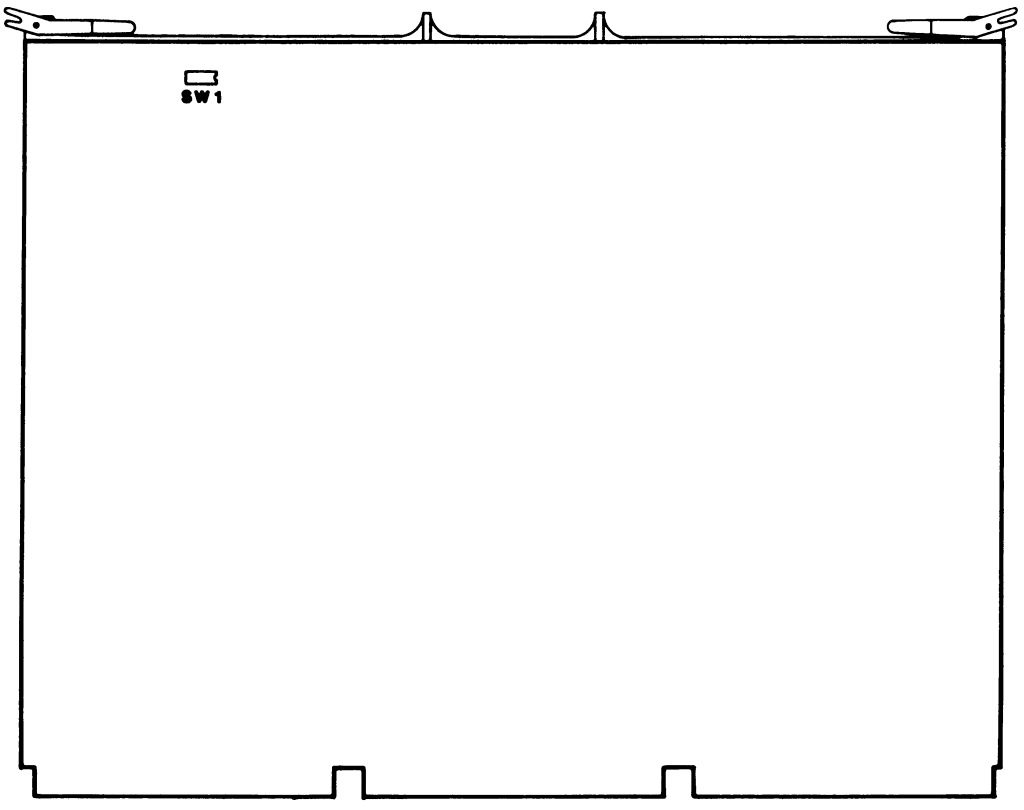
Use Pencil

Figure 5-1. Configuration Record Sheet (SH 2 of 3)

1. Emulation PROM numbers range from _____ to _____

2. Switch settings (circle 1 or 0)





Bus Translator PCBA

Use Pencil

Figure 5-1. Configuration Record Sheet (SH 3 of 3)

5.4 GENERAL FAULT ISOLATION PROCEDURES

The ensuing suggested fault isolation procedures are general in nature, based on established troubleshooting techniques, and should be used primarily as a guide. Following these procedures can aid in determining whether the equipment failure is a result of operator error or equipment malfunction, speed location of a failed circuit component, and minimize down time caused by equipment malfunctions.

5.4.1 ISOLATING THE PROBLEM

In troubleshooting electronic equipment, the problem can usually be attributed to any of three sources:

a. Operator error

b. Adverse environmental factor(s)

c. Equipment malfunction.

Operator error is a more prevalent source of equipment problems than most operators care to admit. Operating procedures should always be investigated and eliminated **BEFORE** assuming any other source of malfunction exists. The symptoms should not be systematically investigated for environmental or electromechanical symptoms of malfunction until all possibility of human error has been eliminated.

5.4.2 OPERATING PROCEDURE CHECK

A system malfunction, appearing to be caused by circuit failure, is often found to be the result of improper operation or application of the equipment. When a problem is observed, the operating procedures being used with the malfunctioning unit and its associated units must therefore be thoroughly checked to ensure they are being correctly performed.

5.4.3 MANUAL OPERATIONS CHECK

A check must be made to determine if manual operations such as cleaning, servicing, or troubleshooting were performed on the equipment or related equipment before the first observed abnormal operation. Recently performed manual operations are suspect and should be double-checked to ensure that they were properly executed. Emulex recommends the following checks:

a. Verify recently changed procedures correctly performed.

b. Verify adjustment settings (if any) properly made.

c. Verify tightness of system connector installations.

d. Verify that any parts temporarily removed or disconnected were properly and securely replaced; this check should include proper seating of PCBAs in slots of CPU backplane. V-MASTER/780, or DEC Expansion Box cabinet.

e. Verify that no accidentally loosened or damaged components are evident. Tighten any loose components and replace any obviously damaged components.

5.4.4 VISUAL INDICATOR CHECK

If the malfunction persists after double-checking all recent manual operations, visually check the status of all operating controls and indicators in the system. Visual indicators include the following items:

a. Switches and indicator lights on PCBAs and operator control panels (OCPs)

b. Busses

c. Switches and/or indicators mounted out of sight on internal chassis or PCBAs

d. Printed data outputs

e. Signals monitored at test points by using meters, oscilloscopes, etc.

Correct any observed control-setting errors. Attempt to determine possible causes of erroneous indication.

5.4.5 POWER CIRCUIT CHECK

The effects of power supply malfunctions are normally widespread, which makes diagnosis of the problem difficult. Error indications tend to appear throughout the equipment and are difficult to localize. These symptoms, however, can sometimes be used as an indication that the cause of the problem is basic and pertains to the power circuits.

5.4.5.1 Fuses/Circuit Breakers

Verify that all fuses or circuit breakers in the power circuits are of the proper type and rating, and that none have blown. This check should include any fuses or circuit breakers internally mounted and not readily accessible from the front or rear of the major units of the system. Remove any blown fuse and replace with new fuse of the same type and rating.

CAUTION

Fuses with higher ratings or faster blow time limits than those removed must **NEVER** be installed. Determine cause of fuse failure and correct problem **BEFORE** replacing failed fuse.

Micro-fuse F1 on the Cable Paddleboard PCBA (P/N SU7810404) is the only fuse in the Emulex system. If blown, -5 Vdc is not available to the SMD interface circuits and the Self-Test cannot be completed. The Self-Test must sence "-5V OK" as part of the check sequence (see subsection 5.5.8).

5.4.5.2 Voltage Levels

Verify that power of the proper frequency and amplitude is being supplied to the equipment. If the primary input power is correct, check the output levels from all internal power supplies. All such outputs must be within required specifications (see applicable technical manuals for the equipment) and not subject to slow or intermittent drifting. If the problem is cyclic or intermittent; i.e., appears for a period of time and then disappears, check the power supplies for extreme sensitivity to variations in ambient temperature (heat or cold).

5.4.6 ELECTRONIC CIRCUIT CHECKS

When the possibility of operator error has been eliminated, and the existing symptoms have been thoroughly analyzed but the cause of the problem cannot be found, then attempt to determine if the problem is repeatable, continuous, or intermittent. The identical operation should be repeated several times to determine the types and number of failures.

If repeating the operation fails to sufficiently isolate the location of the malfunctioning circuit area, all the diagnostic programs should be run to determine if the symptoms appear under all conditions.

The power supply voltages, as well as the AC line voltage at the input, should be checked first to determine if they are within specification. The basic timing circuits should then be checked. Problems in either of these areas are difficult to diagnose, since these circuits affect operation of all other circuits. These timing circuits, in turn, make error indications intermittent and problem isolation difficult. Varying the environment (power supply voltages, heat, mechanical shock, etc.) may sometimes cause an intermittent problem to occur more often so that it can be investigated more effectively.

- - - - - - -
C A U T I O N
- - - - - - -

The +5V should only be varied ±5% in margin tests. The IC chips used are rated from +4.75V to +5.25V.

5.4.6.1 Circuit Divisions

When attempting fault isolation in electronic systems, it is best to divide the system into troubleshooting areas, with each system unit being considered as a separate area. Then each functional section of each unit (power circuits, amplifier circuits, servo circuits, digital circuits, analog circuits, etc.) should be considered as a separate area. In this way, each area can be individually evaluated, and those not involved in the problem can be eliminated from consideration. The source of the problem is thus isolated into ever smaller stress until only the actual problem area remains.

Most electronic equipment operates from an interwoven network of circuits. Malfunctions or improper operating procedures originating in one area of the equipment often cause failure symptoms within that area and other related areas. These symptoms are the foremost troubleshooting aids available and should be used to their fullest extent. In many instances, a malfunction can be isolated to a particular area by completely analyzing the symptoms.

5.4.7 NOISE PROBLEM CHECKS

Many times, equipment failures occur which are extremely intermittent and seem to appear at random intervals. The cause of these symptoms can often be traced to the power ON/OFF switching of heavy machinery or high-powered electrical devices in the immediate area. Such events can cause extreme noise signals on the primary AC power input lines and a sudden variation in line voltage may be reflected in the DC operating voltages which can result in an equipment failure. Therefore, when extremely intermittent failures are encountered, an attempt must be made to reference these failures to a simultaneous outside occurrence which might have a bearing on the problem.

Individual power supplies within the equipment must be checked for excessive ripple in output levels. Checks must also be performed for noise bursts caused by the combination of loose electrical connections and mechanical shock or vibration. In some situations, individual components may also be found to be sensitive to mechanical shock or vibration even though all connections are secure.

5.5 SPECIFIC FAULT ISOLATION PROCEDURES

This subsection describes fault symptoms and causes which the installing technician can easily observe without using special

instruments: FAULT LED ON or blinking, impossible to read contents of SC7000 Disk Controller registers from console, and production of random errors when diagnostics are run.

Symptoms and subsections that explain possible causes and remedies are listed in the following table:

Symptom	Subsection for Possible Cause/Remedy
FAULT LED ON	5.5.1, 5.5.6, 5.5.7, 5.5.8
FAULT LED Blinking	5.5.5
Registers in SC7000 Disk Controller cannot be addressed, or they return unexpected data	5.5.1, 5.5.2, 5.5.3
Diagnostics produce hard and repeatable errors	5.5.1, 5.5.2, 5.5.4
Diagnostics produce random errors	5.5.1, 5.5.2

5.5.1 SBI COAXIAL CABLES

An improperly installed or faulty SBI coaxial cable can be indicated by a range of symptoms from the inability of the SC7000 Disk Controller to pass self-test to the intermittent failure of diagnostics.

5.5.1.1 Improperly Installed SBI Coaxial Cables

The header for each SBI coaxial cable is designed to ensure that a pin is not bent when the header is misaligned. The header does allow a pair of pins to be open above or below the header, as well as an entire row to the left or right of the header. A very careful visual check with a flashlight, while power is off, is strongly advised before power is applied after installation, and at the first sign of trouble.

5.5.1.2 Open SBI Coaxial Cables

The coaxial cable assemblies are subject to internal failure from fatigue or mishandling. If a conductor in one of the cables becomes open, the corresponding signal can not be propagated past the break. A missing signal may prevent the SC7000 Disk Controller from completing self-test or cause errors during verification exercises. A broken conductor downstream from the V-MASTER can also prevent proper termination of that line.

If the SC7000 Disk Controller does not pass self-test (FAULT LED ON), the clock pulses from the SBI bus may not be received. The signal at connector J2, pin 8 on the SC7000 Disk Controller should be checked with an oscilloscope and show a pulse duration period of 150 nanoseconds. Connector J2 is accessible from the front with the SC7000 Disk Controller plugged into the V-MASTER or into the VAX-11/750 CPU backplane. Connector J2 is the top of two sets of pins, with pin 8 being the fourth pin up on the side nearest to the outside. This clock pulse is logically derived on the Bus Translator PCBA (SU7810402) from the four clock lines of the SBI bus. The most common cause for bad clock signals are incorrectly installed SBI cables or terminators (see subsection 5.5.2).

If the diagnostics run with intermittent and random failures, the cause may be related to improper termination of the SBI. Both ends of the SBI bus have PULL UP/PULL DOWN termination resistors: at the extreme left end, the resistors are on a module of the CPU and at the extreme right end, they are on a terminator PCBA. The resistance between ground and every line on the bus, except the four clock lines (PDCLK H/L and PCLK H/L), should be 37 Ohms. If 72 Ohms is measured, that measurement would indicate the line is connected to only one of the two terminating resistors. The clock pulses are terminated only at the terminator (right) end and the resistance between ground and these clock lines should be 72 Ohms. The SBI signal lines are identified on the V-MASTER backplane and in Tables 8-6 and 8-7 for the Bus Interface PCBA and Bus Translator PCBA, respectively.

5.5.2 TERMINATOR PROBLEMS

If the Terminator PCBA is improperly installed, diagnostics may produce intermittent errors. If problems are observed, verify the terminator is properly seated on the Bus-Out pins of the V-MASTER backplane or that the coaxial cables are properly installed on the DEC terminator (see subsection 5.5.1). Also check to verify that no broken coaxial cables are present (see subsection 5.5.1.2). If the visual checks are satisfactory and a terminator problem is still suspected, the following checks can help to isolate the problems.

The terminator PCBA receives power from the main frame power supply. Voltage measured between connector J7, pin 1 on the terminator PCBA and ground should be +5 Vdc; and between pin 3 and ground, voltage should be -5.2 Vdc. System ground for the terminator PCBA is at connector J7, pins 2 and 4.

The main frame power supplies also provide the terminal with an "AC LOW" signal and a "DC LOW" signal. The "AC LOW" signal can be measured on the terminator PCBA at connector J8, pin 1, and at connector J9, pin 1 and have a magnitude of -10 Vdc. The "DC LOW" signal can be measured on the terminator PCBA at connector J8, pin 2, and at connector J9, pin 2 and have a magnitude of -7 to -10 Vdc.System ground for these signals is at connector J8, pin 3, and connector J9, pin 3.

The signal derived from the "DC LOW" signal is "BUS SBI DEAD L" which should have a level of at least +2 Vdc (TTL high) at pin B60 of slot 2 (connector B) on the Bus Translator PCBA in all V-MASTERs in the system.

The signal derived from the "AC LOW" signal is "BUS SBI FAIL L" which should have a level of at least +2 Vdc (TTL high) at pin TT of SBI connector J3-J9 (second from bottom). SBI pin/signal assignments are listed in Table 8-5.

5.5.3 BUS INTERFACE PCBA OR BUS TRANSLATOR PCBA MALFUNCTION

In the V-MASTER VAX-11/780 CPU system, if the SC7000 Disk Controller does not respond when addressed from the console, the cause of the problem may be in the Bus Interface PCBA or in the Bus Translator PCBA instead of in the SC7000 Disk Controller. The data and address paths through those PCBAs may be verified by using the following procedure:

Configure the SC7000 Disk Controller(s) to be in the Forced Reset mode (switch SW5-1 ON), and install them in slots 3 (and 4) of the V-MASTER. When the SC7000 Disk Controller(s) are unable to respond to addresses on the internal bus of the V-MASTER, the address associated with the Examine Controller Register function is echoed back to the console as data; e.g.,

```
>>> E/L/P 20014414
    P 20014414    F0F28414
```

This data is an Examine of the contents of the Disk Address Register (RMDA) of disk drive zero (offset = 414) on TR10 (20014000). The Bus Translator PCBA converts the SBI address to an address which is compatible with the address on the VMI bus of the V-MASTER. If the SC7000 Disk Controller is in slot 3 of the V-MASTER, the address is converted to F0F28XXX. The least significant (LS) three hexadecimal digits of the SBI address are passed through unchanged. With the SC7000 Disk Controller reset and unable to respond, the "data" read by the Examine instruction is F0F28414 which is the correct reflection of the address presented on the VMI bus by the Bus Translator PCBA.

If the SC7000 Disk Controller is in slot 4 with switch SW8-8 ON, the SBI address is translated to F0F2AXXX. Of course, the SBI address used to access the V-MASTER depends on the TR level to which the Bus Interface PCBA is configured.

NOTE

If two SC7000 Disk Controllers are installed in the V-MASTER, the even TR is associated with the SC7000 Disk Controller in slot 3 and the odd TR is associated with the SC7000 Disk Controller in slot 4.

The purpose of this exercise is to determine whether the SBI address is or is not being translated properly. An SC7000 Disk Controller in the V-MASTER would not be expected to respond if the SBI address was not being translated properly.

If a successful examination of the contents of a Controller Register cannot be made, the CPU internal registers should be examined to determine the type of failure:

```
>>> E/I  30
        30   00040000

>>> E/I  34
        34   00008002  (or 00000002)
```

The responses in these two statements indicate no error status.

Internal Register 30, bit 31 most significant bit (MSB) indicates SBI parity error; bit 29 = unexpected read data; bit 27 = multiple-transfer fault; bit 26 = transmit fault; bit 17 = Fault signal.

Internal Register 30 can be cleared by a deposit of "F0000":

```
>>> D/I  30  F0000
```

Internal Register 34, bit 08 indicates CPU confirmation response; bit 06 = bus time out.

Internal Register 34 can be cleared by a deposit of "FFFF":

```
>>> D/I  34  FFFF
```

5.5.4 REVERSED B-CABLE

Read data failures from the disk drive could be caused by a reversed B-Cable. With the disk drive cycled down, remove the A-Cable and the FAULT LED on the SC7000 Disk Controller should blink. If this LED does not blink, one connector of the B-Cable is probably reversed.

5.5.5 DISK DRIVE PROBLEMS

A blinking FAULT LED indicates no disk drive is cabled in and/or powered up.

A slowly blinking FAULT LED indicates two disk drives have been assigned the same disk drive number. The number ID plug or switch setting must be changed on the disk drive.

5.5.6 NO -5.2 VDC

The -5.2 Vdc line from the main frame power supply may not be properly cabled to the V-MASTER chassis. This voltage should be present between pins 1 and 2 of backplane connector J15; or between ground and pins C79 and C82 on the Bus Interface PCBA (slot 1 in V-MASTER); or between ground and pin C79 on the Bus Translator PCBA (slot 2 in V-MASTER).

5.5.7 AC LOW AND DC LOW ASSERTED

AC LOW and DC LOW signals from the power supply may not be pulled to a logical "OK" state of -7 Vdc by the power supply. Check the voltages for these signals on backplane connector J14, pin 1 (PS ACLO H), and pin 2 (PS DCLO H). These signals are also etched to backplane connector J13, pins 1 and 2, respectively. Pin 3 is ground on both connectors J13 and J14.

5.5.8 CABLE PADDLEBOARD PCBA NOT INSTALLED OR INCORRECTLY INSTALLED

Minus 5 Vdc is supplied by the power converter pack on the rear-mounted Cable Paddleboard PCBA. The SELF-TEST firmware of the SC7000 Disk Controller, which starts on power up, searches for the presence of -5 Vdc as part of the Self-Test function. The FAULT LED remains lit until all tests have been successfully completed. Verify backplane pins are aligned with the Cable Paddleboard PCBA sockets and that this PCBA is inserted flush to the backplane surface. The -5 Vdc can be measured between ground and pins B89 and B91 on the SC7000 Disk Controller PCBA (see Table 8-4), and between ground and pin 9 of ICs U1 through U5 on the Cable Paddleboard PCBA.

5.5.9 FAULT ISOLATION GUIDE

Table 5-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the SC7000 Disk Controller system. It lists possible symptoms, probable cause of the malfunction, and corrective actions.

Table 5-1. SC7000 Disk Controller Fault Isolation Guide

Symptom	Probable Cause	Remedy
CPU powered up, FAULT LED indicator lit.	Self-Test failure.	Verify SC7000 Disk Controller PCBAs are properly seated in CPU backplane, V-MASTER/780 backplane, or DEC Expansion Box backplane. Defective unit. Return SC7000 Disk Controller to factory.
Data Transfer operation attempted but ACTIVITY LED indicator not lit.	A-Cable or B-Cable connector(s) reversed.	Check cable connections and reverse if pins of connectors not properly matched.
	A-Cable or B-Cable to/from addressed disk drive not connected.	Connect cables to/from addressed disk drive.
	Addressed disk drive does not have Ready status.	Perform operations on disk drive that are needed to produce Ready status condition.
	Wrong Base Address coded in configur-ation DIP switches.	Encode correct Base Address in configuration DIP switch pack.
Unable Interrupt CPU	Wrong Interrupt Vector Address coded in configuration DIP switch pack.	Encode correct Interrupt Vector Address in configuration DIP switch pack.

Other procedures for isolating fault symptoms and causes are presented in subsections 5.5.1 through 5.5.8.

BLANK

6.1 OVERVIEW

This section describes and defines the bit functions in the various registers, describes commands, and explains programming concepts used with the SC7000 Disk Controller system. This section is divided into six subsections, as listed in the following table:

Subsection	Title
6.1	Overview
6.2	MBA Registers (VAX-11/780)
6.3	MBA Registers (VAX-11/750)
6.4	Device Registers (VAX-11/780 and VAX-11/750)
6.5	Commands
6.6	Programming Information

6.2 MBA REGISTERS (VAX-11/780)

The SC7000 Disk Controller contains eight Massbus Adapter (MBA) registers that are used to interface the SC7000 Disk Controller with the CPU. To initiate disk drive commands, set-up for DMA Data Transfer operations, and monitor status and error conditions, the registers are loaded (written into) and/or read under program control. The MBA registers are read from and written to as long words.

The SC7000 Disk Controller also contains 256 map registers which control the virtual-to-physical mapping for DMA Data Transfer operations.

This subsection shows the format of each of the MBA registers and explains the use and the meaning of each of the bits. The addresses for the registers are for the first MBA, and they are shown in hexadecimal offsets from the Base Address. See Appendix D for the relationship of the Base Address to the TR level and for offsets for additional MBAs.

For quick reference, Figure 6-1 shows the entire MBA register set for the VAX-11/780 configuration. Their mnemonic symbols begin with MBA.

6.2.1 MBA CONFIGURATION/STATUS REGISTER (MBACSR) **Base Address + 00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WDS	URD	0	MT	XF	0	0	PD	PU	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

6.2.2 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MMM	IE	ABT	INIT

6.2.3 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	RDS	ITO	RTO

6.2.4 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select (MS)								Byte Offset							

Figure 6-1. SC7000 Disk Controller MBA Register Set for VAX-11/780 (SH 1 of 3)

6.2.5 MBA BYTE COUNTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Disk Drive Byte Count															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI Byte Count															

6.2.6 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MFAIL		MWCK	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2.7 MBA SELECTED MAP REGISTER (MBASMR) **Base Address + 18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	0	0	0	0	0	0	0	0					

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Page Frame Number															

6.2.8 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Control				VMI Physical Address											

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VMI Physical Address															

Figure 6-1. SC7000 Disk Controller MBA Register Set for VAX-11/780 (SH 2 of 3)

6.2.9 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0					

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Page Frame Number															

Figure 6-1. SC7000 Disk Controller MBA Register Set for VAX-11/780 (SH 3 of 3)

NOTE

In the description of register contents, no bit positions filled by a zero are described unless the zero(s) represent part of a code.

6.2.1 MBA CONFIGURATION/STATUS REGISTER (MBACSR) **Base Address + 00**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WDS	URD	0	MT	XF	0	0	PD	PU	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SBI Parity Error (PE) - Bit 31

This bit is set when an SBI parity error is detected. It is cleared by power failure or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Write Data Sequence (WDS) - Bit 30

This bit is set when no write data is received after a Write command has been issued. It is cleared by the Power Fail signal or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Unexpected Read Data (URD) - Bit 29

This bit is set when unexpected read data is received. It is cleared by the Power Fail signal or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Multiple Transfer (MT) - Bit 27

This bit is set when the ID on the SBI does not agree with the transmitted ID while the SC7000 Disk Controller is transmitting information on the SBI. It is cleared by power failure or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Transmit Fault (XF) - Bit 26

This bit is set when SBI Fault signal is detected while the SC7000 Disk Controller is transmitting information on the bus. It is cleared by power failure or by de-assertion of the Fault signal.

Controller Power Down (PD) - Bit 23

This bit is set when the SC7000 Disk Controller receives an asserted AC LO signal. It is cleared when power to the SC7000 Disk Controller goes up, or by assertion of INIT, UNJAM, or DC LO signals, or by writing a one into this bit position. Setting this bit causes an Interrupt to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Controller Power Up (PU) - Bit 22

This bit is set when the SC7000 Disk Controller receives de-assertion of the AC LO signal. It is cleared when power to the SC7000 Disk Controller goes down, or by assertion of INIT, UNJAM, or DC LO, or by writing a one into this bit position. Setting this bit also sets the IE bit (MBACR bit 02) and causes an Interrupt to be sent to the CPU.

Adapter Code - Bits <07:00>

Each type of Massbus Adapter (MBA) is assigned a unique code to identify it. The code for this MBA device is 00100000.

6.2.2 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MMM	IE	ABT	INIT

This register provides four control bits for the MBA functions of the SC7000 Disk Controller. All bits are cleared by the asserted INIT signal.

MBA Maintenance Mode (MMM) - Bit 03

This bit is set to place the SC7000 Disk Controller in the Maintenance mode. The SC7000 Disk Controller cannot be placed in the Maintenance mode while a Data Transfer operation is in progress. The Maintenance mode established by this set bit is only partially emulated.

Interrupt Enable (IE) - Bit 02

When this bit is set, the SC7000 Disk Controller can interrupt the CPU when certain conditions occur. It is cleared by writing a zero into this bit position, or by an asserted INIT or UNJAM signal.

Abort (ABT) - Bit 01

Setting this bit initiates the Data Transfer Abort sequence which stops the Data Transfer operation and causes an Interrupt to the CPU if the IE bit is set.

Initialize (INIT) - Bit 00

Setting this bit clears the SC7000 Disk Controller of any pending commands, aborts any Data Transfer operation in progress, and clears all registers, including this bit position (see subsection 6.4.1).

6.2.3 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	RDS	ITO	RTO

All bits in this register, except DTB, NED and ATTN, are cleared by writing a one into the bit position, or by setting the INIT bit (MBACR bit 00), or by subsequent receipt of a valid Data Transfer command.

Data Transfer Busy (DTB) - Bit 31

This Read-only bit is set when a Data Transfer command is received. It is cleared when the Data Transfer operation is terminated normally or when the Data Transfer operation is aborted. No Interrupt can occur if DTB is set to logic one.

No Response Confirmation (NRC) - Bit 30

This bit is set when the SC7000 Disk Controller receives no response confirmation for the command or write data sent on the SBI. Setting this bit causes a retry of the command.

Corrected Read Data (CRD) - Bit 29

This bit is set when data received from memory has been corrected.

Programming Error (PGE) - Bit 19

This bit is set when there exists one or more of the following conditions:

a. Program tries to initiate a Data Transfer operation when the SC7000 Disk Controller is currently performing a Data Transfer operation.

b. Program tries to load MBAVAR, MBABC, or Map registers while the SC7000 Disk Controller is currently performing a Data Transfer operation.

c. Program tries to establish Maintenance mode while the SC7000 Disk Controller is currently performing a Data Transfer operation.

When this bit is set, the Data Transfer operation is not aborted. If bit IE is set to logic one, then an Interrupt occurs at the end of the Data Transfer operation. Since the Interrupt is caused by completion of the Data Transfer operation, PGE set does not cause the Interrupt condition but does retain the Interrupt condition if it is not cleared and if bit IE remains set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses any disk drive register for a disk drive that does not exist. Setting this bit sends zero disk drive data back to the CPU and causes an Interrupt to the CPU if the IE bit is set.

Massbus Control Bus Parity Error (MCPE) - Bit 17

This bit is set when NED is set.

Attention (ATTN) - Bit 16

This Read-only bit is asserted if any of the Attention Active (ATA) bits in register RMAS are asserted. Asserting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Transfer Completed (DTC) - Bit 13

This bit is set whenever a Data Transfer operation is terminated because of normal completion or because of an error condition. Setting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when a Data Transfer operation is aborted for any reason. Setting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Late (DLT) - Bit 11

This bit is set during a Read operation if the data buffer overflows, or during a Write or Write Check operation if the data buffer underflows. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a Compare error is detected in the upper byte while the SC7000 Disk Controller is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a Compare error is detected in the lower byte while the SC7000 Disk Controller is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Missed Transfer Error (MXE) - Bit 08

This bit is set when there exists one or more of the following conditions:

a. An illegal command in the range from 2D to 3F is received; ILF (RMER1 bit 00) is set.

b. A Data Transfer operation is attempted while ERR is set, MOL is cleared, or VV is cleared (RMDS bits 14, 12, and 06, respectively). IVC (RMER2 bit 12) is set.

Setting this bit aborts the Data Transfer operation that is currently in progress.

Exception (EXC) - Bit 07

This bit is set to indicate an Error condition was detected during a Data Transfer operation between the SC7000 Disk Controller and

the selected disk drive. Setting this bit aborts the Data Transfer operation that is currently in progress.

Invalid Map (IM) - Bit 04

This bit is set when the Valid (V) bit of the next page frame number is zero and the byte count is not zero. Setting this bit aborts the Data Transfer operation that is currently in progress.

Error Confirmation (EC) - Bit 03

This bit is set when the SC7000 Disk Controller receives a bus error confirmation for a Read or Write command. Setting this bit aborts the Data Transfer operation that is currently in progress.

Read Data Substitute (RDS) - Bit 02

This bit is set when the Read Data received from memory is indicated to be Read Data Substitute. Setting this bit aborts the Data Transfer operation that is currently in progress.

Interface Sequence Timeout (ITO) - Bit 01

This bit is set when the SC7000 Disk Controller receives a bus error confirmation, or when it fails to receive response confirmation before 102.4 microseconds have elapsed after the command was initially sent on the SBI. Setting this bit aborts the Data Transfer operation that is currently in progress.

Read Data Timeout (RTO) - Bit 00

This bit is set when the SC7000 Disk Controller fails to receive Read Data before 102.4 microseconds have elapsed after the Read command was initially sent on the SBI. Setting this bit aborts the Data Transfer operation that is currently in progress.

6.2.4 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select							Byte Offset								

This register contains the 17-bit Virtual Address for the Data Transfer operation. Bits <08:00> select the byte within the page, and bits <16:09> select one of the 256 Map registers. The 9-bit byte offset field, minus the two least significant bits, is concatinated with the 21-bit physical page address obtained from the addressed Map register to form the 28-bit physical VMI address.

The Virtual Address is incremented by four after every memory Read or Write operation, and does not point to the next byte to be transferred unless the Data Transfer operation ends on a longword boundary. Also, when a Write Check error is detected, the MBAVAR does not point to the failing memory address because the data buffer is preloaded. The Virtual Address of the bad data may be determined from the number of bytes actually transferred by the disk drive and adding that number of bytes to the initial Virtual Address.

6.2.5 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Disk Drive Byte Count															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI Byte Count															

This register contains the byte count for the number of bytes transferred to or from the selected disk drive and the number of bytes transferred to or from memory. Each byte transfer stops when the respective byte count reaches zero. The program initially loads the two's complement of the number of bytes for the Data Transfer operation into bits <15:00> of this register. The SC7000 Disk Controller then loads this value into bits <31:16> of this register.

6.2.6 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MFAIL	MWCK		
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register cannot be written into unless MMM (MBACR bit 03) is set. Unless explicitly written into, this register contains 'BF' for data. It is cleared to contain 'BF' whenever an INIT sequence is executed. Only bits <31:21> are Read/Write; all other bits are Read-only. The SC7000 Disk Controller emulates only the following bits:

Simulated SCLK (SSCK) - Bit 27

Setting this bit sets MWCK (bit 18).

Simulated ATTN (SATN) - Bit 24

Setting this bit sets ATTN (MBASR bit 16).

Massbus Fail (MFAIL) - Bit 20

This bit status reflects the status of MMM (MBACR bit 03).

Maintenance Write Clock (MWCK) - Bit 18

This bit status reflects the status of SSCK (bit 27).

6.2.7 MBA SELECTED MAP REGISTER (MBASMR) **Base Address + 18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	0	0	0	0	0	0	0	0	0	0					
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Page Frame Number															

Bits <20:00> in this register contain contents of the map register pointed to by MBAVAR bits <16:09>. Bit 31 equals logic one because only the last valid map register used during a DMA is loaded here.

6.2.8 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Control				VMI Physical Address											
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VMI Physical Address															

The contents of this Read-only register are valid during and after a DMA operation. This register contains the byte controls and the VMI Physical Address of the last DMA Data Transfer operation.

6.2.9 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0					
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Page Frame Number															

The SC7000 Disk Controller contains 256 Map registers which are used to form the SBI Physical memory Address from the 17-bit Virtual Address contained in register MBAVAR. Map registers can be written into only when no Data Transfer operation is in progress. An attempt to write into a Map register during a Data Transfer operation is ignored and sets PGE (MBASR bit 19).

Valid Bit (V) - Bit 31

The set status of this bit indicates the entry is a valid Page Frame Number (PFN). If this bit is not set and the DMA operation attempts to use a Map register, the IM bit (MBASR bit 04) is set to indicate an error (see subsection 6.2.3).

Physical Page Frame Number (PFN) - Bits <20:00>

This field contains the high-order 21 bits of the Physical Memory Address.

6.3 MBA REGISTERS (VAX-11/750)

The SC7000 Disk Controller contains seven MBA registers. The first MBA register is not used in the VAX-11/750 CPU system and returns all zeros when its contents are read. Register MBASMR does not exist in the VAX-11/750. The MBA registers are used to interface the SC7000 Disk Controller with the CPU. To initiate disk drive commands, set-up for DMA Data Transfer operations, and monitor status and error conditions, the registers are loaded (written into) and/or read from under program control. The MBA registers are read from and written to as long words.

The SC7000 Disk Controller also contains 256 Map registers which control the Virtual-to-Physical mapping for DMA Data Transfer operations.

This subsection shows the format of each of the MBA registers and explains the use and the meaning of each of the bits. The addresses for the registers are for the first MBA and they are shown in hexadecimal offsets from the Base Address. See Appendix D for the relationship of the Base Address to the MBA level and for offsets for additional MBAs.

For quick reference, Figure 6-2 shows the entire MBA register set for the VAX-11/750 configuration. Their mnemonic symbols begin with MBA.

6.3.1 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	IBC	MMM	IE	ABT	INIT

6.3.2 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	0	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	0	NRS	0

6.3.3 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address +0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0								MS
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select (MS)							Byte Offset								

Figure 6-2. SC7000 Disk Controller MBA Register Set for VAX-11/750 (SH 1 of 2)

6.3.4 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Disk Drive Byte Count															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMI Byte Count															

6.3.5 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MFAIL	MWCK		
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3.6 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				Operation			0	Physical Address							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Address															

6.3.7 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Physical Page Frame Number														

Figure 6-2. SC7000 Disk Controller MBA Register Set for VAX-11/750 (SH 2 of 2)

6.3.1 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	IBC	MMM	IE	ABT	INIT

This register provides five control bits for the MBA functions of the SC7000 Disk Controller. All bits are cleared by the asserted INIT signal.

Ignore Byte Count Mode (IBC) - Bit 04

When this bit is set, a Data Transfer operation is not terminated by the byte counter overflow. If the IE bit is set, an Interrupt is generated each time the byte counter overflows. This bit cannot be set while a Data Transfer operation is in progress.

MBA Maintenance Mode (MMM) - Bit 03

This bit is set to place the SC7000 Disk Controller in the Maintenance mode. The SC7000 Disk Controller cannot be placed in the Maintenance mode while a Data Transfer operation is in progress. The Maintenance mode is only partially emulated.

Interrupt Enable (IE) - Bit 02

When this bit is set, the SC7000 Disk Controller can interrupt the CPU when certain conditions occur. It is cleared by writing a zero into this bit position, or by an asserted INIT signal.

Abort (ABT) - Bit 01

Setting this bit initiates the Data Transfer Abort sequence which stops the Data Transfer operation and causes an Interrupt to the CPU if the IE bit is set.

Initialize (INIT) - Bit 00

Setting this bit clears the SC7000 Disk Controller of any pending commands, aborts any Data Transfer operation in progress, and clears all registers, including this bit position (see subsection 6.5.1).

6.3.2 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	0	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	0	NRS	0

In this register, all bits except DTB, NED, and ATTN, are cleared by writing a one into the bit position, or by setting the INIT bit (MBACR bit 00), or by subsequent receipt of a valid Data Transfer command.

Data Transfer Busy (DTB) - Bit 31

This Read-only bit is set when a Data Transfer command is received. It is cleared when the Data Transfer operation is terminated normally or when the Data Transfer operation is aborted. No Interrupt can occur if DBY is set to logic one, unless the byte count overflows to zero while bit IBC (MBACR bit 04) is set.

Corrected Read Data (CRD) - Bit 29

This bit is set when data received from memory has been corrected.

Programming Error (PGE) - Bit 19

This bit is set when there exists one or more of the following conditions:

a. Program tries to initiate a Data Transfer operation when the SC7000 Disk Controller is currently performing a Data Transfer operation.

b. Program tries to load MBAVAR, MBABC or Map registers while the SC7000 Disk Controller is currently performing a Data Transfer operation and bit IBC is reset.

c. Program tries to establish Maintenance mode while the SC7000 Disk Controller is currently performing a Data Transfer operation.

When this bit is set, the Data Transfer operation is not aborted. If bit IE is set to logic one, then an Interrupt occurs at the end of the Data Transfer operation. Since the Interrupt is caused by completion of the Data Transfer operation, PGE set does not cause the Interrupt condition but does retain the Interrupt condition if it is not cleared and if bit IE remains set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses any disk drive register for a disk drive that does not exist. Setting this bit sends zero disk drive data back to the CPU and causes an Interrupt to the CPU if the IE bit is set.

Massbus Control Bus Parity Error (MCPE) - Bit 17

This bit is set when NED is set.

Attention (ATTN) - Bit 16

This Read-only bit is asserted if any of the Attention Active (ATA) bits in register RMAS are asserted to indicate a disk drive requires attention. When this bit is set, an Interrupt is sent to the CPU if the IE bit is set.

Data Transfer Completed (DTC) - Bit 13

This bit is set whenever a Data Transfer operation is terminated because of normal completion or because of an error condition. Setting this bit causes an interrupt to the CPU if the IE bit is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when a Data Transfer operation is aborted for any reason. Setting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Late (DLT) - Bit 11

This bit is set during a Read operation if the data buffer overflows, or during a Write or Write Check operation if the data buffer underflows. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a Compare error is detected in the upper byte while the SC7000 Disk Controller is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a Compare error is detected in the lower byte wgile the SC7000 Disk Controller is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Missed Transfer Error (MXE) - Bit 08

This bit is set when there exists one or more of the following conditions:

a. An illegal command in the range from 2D to 3F is received. Bit ILF (RMER1 bit 00) is set.

b. A Data Transfer operation is attempted while ERR is set, MOL is cleared, or VV is cleared (RMDS bits 14, 12, and 06, respectively). Bit IVC (RMER2 bit 12) is set.

Setting this bit aborts the Data Transfer operation that is currently in progress.

Exception (EXC) - Bit 07

This bit is set to indicate an error condition was detected during a Data Transfer operation between the SC7000 Disk Controller and the selected disk drive. Setting this bit aborts the Data Transfer operation that is currently in progress.

Invalid Map (IM) - Bit 04

This bit is set when the valid bit of the next page frame number is zero and the byte count is not zero. Setting this bit aborts the Data Transfer operation that is currently in progress.

Error Confirmation (EC) - Bit 03

This bit is set when the SC7000 Disk Controller receives a bus error confirmation for a Read or Write command. Setting this bit aborts the Data Transfer operation that is currently in progress.

No Response Status (NRS) - Bit 01

This bit is set when the SC7000 Disk Controller receives no response from memory during a DMA Data Transfer operation. It indicates the effective physical memory address was non-existent. Setting this bit aborts the Data Transfer operation that is currently in progress.

6.3.3 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0								
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select							Byte Offset								

This 24-bit register contains the 17-bit Virtual Address for the Data Transfer operation. Bits <08:00> select the byte within the page, and bits <16:09> select one of the 256 Map registers. Bits <23:17> can be written to or read from, but they have no function or affect. The nine bits of the Byte Offset field are concatinated with the 15-bit Physical Page Address obtained from the addressed Map register to form the 24-bit physical CMI address. The Virtual Address is incremented by four after every memory Read or Write operation and does not point to the next byte to be transferred if the Data Transfer operation does not end on a longword boundary. Also, when the SC7000 Disk Controller detects a Write Check Error, register MBAVAR does not point to the failing Memory Address because the data buffer is preloaded. The Virtual Address of the bad data may be determined from the number of bytes actually transferred by the disk drive and adding that number of bytes to the initial Virtual address.

6.3.4 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Disk Drive Byte Count															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMI Byte Count															

This register contains the byte count for the number of bytes transferred to or from the selected disk drive and the number of bytes transferred to or from memory. Each byte transfer stops when the respective byte count reaches zero. The program initially loads the two's complement of the number of bytes for the Data Transfer operation into bits <15:00> of this register. The SC7000 Disk Controller then loads this value into bits <31:16> of this register.

6.3.5 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MFAIL	MWCK		
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register cannot be written into unless MMM (MBACR bit 03) is set. Unless explicitly written into, this register contains 'BF' for data. It is cleared to contain 'BF' whenever an INIT sequence is executed. Only bits <31:21> are Read/Write; all other bits are

Read-only. The SC7000 Disk Controller emulates only the following bits:

Simulated SCLK (SSCK) - Bit 27

Setting this bit sets MWCK (bit 18).

Simulated ATTN (SATN) - Bit 24

Setting this bit sets ATTN (MBASR bit 16).

Massbus Fail (MFAIL) - Bit 20

This bit status reflects the status of MMM (MBACR) bit 03).

Maintenance Write Clock (MWCK) - Bit 18

This bit status reflects the status of SSCK (bit 27).

6.3.6 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				Operation			0	Physical Address							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Address															

The contents of this Read-only register are valid during and immediately after a DMA Data Transfer operation. This register contains the byte mask, operation code, and physical address of the last DMA Data Transfer operation.

6.3.7 MBA MAP REGISTERS **Base Address + <800: 8FC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	Physical Page Frame Number														

The SC7000 Disk Controller contains 256 Map registers which are used to form the CMI physical memory address from the 17-bit Virtual Address contained in register MBAVAR. Map registers can be written into only when no Data Transfer operation is in progress.

An attempt to write into a Map register during a Data Transfer operation with bit IBC (MBACR bit 04) reset is ignored and sets PGE (MBASR bit 19).

Valid Bit (V) - Bit 31

The set status of this bit indicates the entry is a valid Page Frame Number (PFN). If this bit is not set and the DMA operation attempts to use a Map register, the IM bit (MBASR bit 04) is set to indicate an error (see subsection 6.3.2).

Physical Page Frame Number (PFN) - Bits <14:00>

This field contains the high-order 15 bits of the Physical Memory Address.

6.4 DEVICE REGISTERS

The SC7000 Disk Controller contains 16 accessible device registers for each of the logical disk drive units. These registers are read from and written to as long words and return the upper half of register MBASR in bits <31:16> when read. The addresses for the device registers are for logical disk drive unit zero, and they are shown in hexadecimal offsets from the Base Address. See Appendix D for the relationship of the Base Address to the TR level and for additional offsets.

For quick reference, Figure 6-3 shows the entire device register set for both VAX-11/780 and VAX-11/750 CPU configurations. All device registers have mnemonic symbols beginning with RM.

6.4.1 CONTROL/STATUS REGISTER 1 (RMCS1) **Base Address + 400**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	DVA	0	0	0	0	0	F4	F3	F2	F1	F0	GO

6.4.2 DRIVE STATUS REGISTER (RMDS) **Base Address + 404**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

6.4.3 ERROR REGISTER 1 (RMER1) **Base Address + 408**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

Figure 6-3. SC7000 Disk Controller Device Register Set (SH 1 of 3)

6.4.4 MAINTENANCE REGISTER 1 (RMMR1) **Base Address + 40C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

6.4.5 ATTENTION SUMMARY REGISTER (RMAS) **Base Address + 410**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

6.4.6 DISK ADDRESS REGISTER (RMDA) **Base Address + 414**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

6.4.7 DRIVE TYPE REGISTER (RMDT) **Base Address + 418**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

6.4.8 LOOK-AHEAD REGISTER (RMLA) **Base Address + 41C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Sector Counter										0	0	0	0	0	0

6.4.9 SERIAL NUMBER REGISTER (RMSN) **Base Address + 420**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW7 -8	SW7 -7	SW7 -6	SW7 -5	SW7 -4	SW7 -3	SW7 -2	SW7 -1	Firmware Revision				Port Number			

6.4.10 OFFSET REGISTER (RMOF) **Base Address + 424**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	SSEI	0	OFD	0	0	0	0	0	0	0

Figure 6-3. SC7000 Disk Controller Device Register Set (SH 2 of 3)

6.4.11 DESIRED CYLINDER REGISTER (RMDC) **Base Address + 428**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Desired Cylinder Address															

6.4.12 HOLDING REGISTER (RMHR) **Base Address + 42C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4.13 MAINTENANCE REGISTER 2 (RMMR2) **Base Address + 430**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
13FF															

6.4.14 ERROR REGISTER 2 (RMER2) **Base Address + 434**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

6.4.15 ECC POSITION REGISTER (RMEC1) **Base Address + 438**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

6.4.16 ECC PATTERN REGISTER (RMEC2) **Base Address + 43C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

6.4.17 ILLEGAL DRIVE REGISTERS **Base Address + <440:47C>**

(Not shown)

Figure 6-3. SC7000 Disk Controller Device Register Set (SH 3 of 3)

6.4.1 CONTROL/STATUS REGISTER 1 (RMCS1) **Base Address + 400**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	DVA	0	0	0	0	0	F4	F3	F2	F1	F0	GO

This Read/Write register is used to store the current disk drive command function code. Setting the GO bit causes the SC7000 Disk Controller to recognize the function code in this register and to initiate the operation for the corresponding disk drive. The actual start of command execution does not begin when GO is set; it starts when the SC7000 Disk Controller has finished any previous operation and then detects a command, which needs initiation, while polling through the disk drive RMCS1 registers.

Drive Available (DVA) - Bit 11

This Read-only bit is set when the polled disk drive is seized by the SC7000 Disk Controller. When not in Dual-Port mode, the disk drive is seized as long as it is powered-up.

Function Code (F4-F0) - Bits <05:01>

Bits F4 through F0 and the GO bit make up the function (command) code which determines the operation to be performed by the SC7000 Disk Controller and selected disk drive. The function codes are listed in the Following table:

Code	Function	Code	Function
01	No Operation	19	Search Command
05	Seek Command	29	Write Check Data
07	Recalibrate	2B	Write Check Header and Data
09	Drive Clear	31	Write Data
0B	Release	33	Write Header and Data
0D	Offset Command	39	Read Data
0F	Return to Centerline	3B	Read Header and Data
11	Read-In Preset	3F	Format (Nonstandard)
13	Pack Acknowledge		

Go (GO) - Bit 00

The GO bit must be set to cause the SC7000 Disk Controller to respond to a command. The GO bit is reset (cleared) after command termination. Nonstandard commands are valid only after the SC7000 Disk Controller has been conditioned to recognize them (see subsection 6.5.4).

6.4.2 DRIVE STATUS REGISTER (RMDS) **Base Address + 404**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This Read-only register contains various status indicators for the addressed disk drive.

Attention Active (ATA) - Bit 15

An Attention condition sets the ATA bit in this register, the corresponding ATA bit in register RMAS, and the composite ATTN bit in register MBASR. This bit is cleared by an INIT sequence, by loading a command with GO (RMCS1 bit 00) set, or by loading a one bit in register RMAS which correlates to the bit position that represents the logical disk drive unit number of the selected disk drive. The last-mentioned method of clearing the ATA bit does not clear the error indicators if any of them are set.

An Attention condition is caused by any of the following conditions:

a. An error in either of the error registers.

b. Completion of a Positioning operation.

c. Status change of MOL (bit 12).

d. Dual-Port operation with the disk drive presently available if previously not available.

e. Correct sector identification for the Search command.

Error (ERR) - Bit 14

This bit is set when one or more of the error bits in Error registers RMER1 and RMER2 for a selected disk drive is set. While ERR is asserted, all commands except Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

This bit is set when a Positioning command is accepted. Positioning commands are: Seek, Recalibrate, and Search. This bit is cleared when the movement function is completed at the time the DRY and ATA bits (bits 07 and 15, respectively) are set. For RM03/RM05 emulations, this bit is set when MOL (bit 12) is reset. This bit is also set during an implied or mid-transfer Seek operation conducted during a Data Transfer operation.

Medium On-Line (MOL) - Bit 12

This bit is set when the Unit Ready line from the selected disk drive is asserted to indicate the disk drive is up to speed, the heads are positioned over the recording tracks, and no Fault condition exists within the disk drive. It is cleared when the disk drive is powered down (spindle stops rotating), or when the disk drive is placed in the Off-Line mode. Whenever the MOL bit changes status, the ATA bit is set. When MOL changes fom a reset to a set condition, bit VV (bit 06) is reset.

Write-Lock (WRL) - Bit 11

This bit is set when the Write Protected line from the selected disk drive is asserted (enabled by a switch located on the disk drive). A Write command to a Write-Locked disk drive causes the Write-Lock Error (WLE) bit (RMERl bit 11) to be set. For RM80 emulations, this bit is set when MOL is reset.

Last Sector Transfer (LST) - Bit 10

This bit is set when the contents of the last addressable sector on the selected disk pack have been read or written. It is cleared when a new address is loaded into register RMDA..

When LST is set, register RMDA is reset to zero and register RMDC increments by one to the first illegal cylinder address. If the byte count is not zero, a mid-transfer Seek operation is aborted. Aborting of the mid-transfer Seek sets status bit AOE (RMERl bit 09) to indicate register RMDC overflowed during a Read or Write operation.

Programmagle (PGM) - Bit 09

This bit is set when Dual-Port or Dual-Access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the SC7000 Disk Controller has seized the selected disk drive. It is reset when the other SC7000 Disk Controller has seized that disk drive. The status of this bit is a reflection of the DVA bit (RMCSl bit 11).

Drive Ready (DRY) - Bit 07

This bit is set at the completion of every command and cleared at the initiation of a command. When set, it indicates the readiness of the selected disk drive to accept a command. If a mechanical motion command was initiated, the ATA bit is also set when DRY is set. This bit is the complement of the disk drive's GO bit.

Volume Valid (VV) - Bit 06

This bit is set by the Pack Acknowledge command or by the Read-In Preset command. It is cleared whenever the disk drive cycles up from the OFF state. When this bit is reset, it indicates the disk drive has been in the Off-Line mode and that a disk pack or cartridge may have been changed.

Offset Mode (OFM) - Bit 00

This bit is set by the Offset command to indicate a Read operation is to be done with the heads in the offset position, as determined by the status of bit OFD (RMOF bit 07). It is cleared by a Read-In Preset, Return-to-Centerline, Recalibrate, or Write command, or by a mid-transfer Seek operation. It is also cleared whenever the disk drive cycles up.

6.4.3 ERROR REGISTER 1 (RMER1) **Base Address + 408**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

This Read/Write register is used to store error status information for the addressed disk drive. If the program attempts to write into this register while the addressed disk drive is busy, bit RMR is set and the contents of this register are not otherwise modified. Writing zeros into this register should not be used as the normal way of clearing errors; instead, the Drive Clear command should be used. When any bit in this register is set, the GO bit is cleared and the DRY bit is set.

Data Check (DCK) - Bit 15

This bit is set when the ECC hardware detects an ECC error during a Read operation. If bit ECI (RMOF bit 11) is not set, the SC7000 Disk Controller performs the error-correction process and bit DRY (RMDS bit 07) is not set until the end of the process. If bit ECI is set, the error-correction process is inhibited, and bit DRY is set immediately. For either of these conditions, the Read operation terminates with the current sector.

Unsafe (UNS) - Bit 14

The status of this bit is a composite reflection of the Power Unsafe and Seek Incomplete error conditions (RMER2 bits 14, 08 and 06). With UNS set, correct results on any operation cannot be guaranteed. Some fault conditions must be cleared by manual intervention on the addressed disk drive.

Operation Incomplete (OPI) - Bit 13

This bit is set when there exists any one of three conditions:

a. A Read or Write command that involves a header search cannot find the physical sector before the SC7000 Disk Controller has detected three Index pulses.

b. During a Search operation, a sector count match is not made before the SC7000 Disk Controller has detected three Index pulses.

c. In Dual-Port mode, a Seek, Search, or Data Transfer command is issued to a disk drive that is busy.

When this bit is set, the GO bit is cleared and the DRY bit is set.

Drive Timing Error (DTE) - Bit 12

This bit is set when either the header or data synchronization (sync) pattern is not found. DTE is also set if the SC7000 Disk Controller detects a Sector pulse before the end of the data field has been reached.

Write Lock Error (WLE) - Bit 11

This bit is set when a Write command is issued to a Write-Locked disk drive.

Invalid Address Error (IAE) - Bit 10

This bit is set when the address is register RMDC and/or RMDA is not valid and an attempt is made to initiate a Seek, Search or Data Transfer command.

Address Overflow Error (AOE) - Bit 09

During a Read or Write operation, bit AOE is set when register RMDC overflows to indicate the address has exceeded the Cylinder Address limit. When bit AOE is set., the SC7000 Disk Controller terminates the operation when the last sector of the last addressed cylinder has been written or read.

Header CRC Error (HCRC) - Bit 08

This bit is set when the SC7000 Disk Controller detects a CRC error in the header. If a Header CRC error is detected during an attempt to perform a Read or Write command, the SC7000 Disk Controller does not perform the Data Transfer operation. If a CRC error occurs during a Read/Write-Check Header and Data command, the contents of the entire sector (including the header) are transferred and the HCRC bit is set.

Header Compare Error (HCE) - Bit 07

This bit is set when the first two words of the header are read from the sector whose sector count is equal to the desired sector field of register RMDA, but does not match the contents of registers RMDC and RMDA. If bit HCE is set during a Read or Write command, the SC7000 Disk Controller does not perform any Data Transfer operation. If bit HCE is set during a Read/Write-Check Header and Data command, the contents of the entire sector (including the header) are transferred and the HCE bit is set.

ECC Hard Error (ECH) - Bit 06

This bit is set when the Error Correction procedure indicates the detected error was an uncorrectable ECC error. DCK (bit 15) is also set when ECH is set.

Write Clock Fail (WCF) - Bit 05

This bit normally contains a zero unless a one is written to it.

Format Error (FER) - Bit 04

This bit is set if bit FMT16 (RMOF bit 12) does not match the state of bit 12 in Word 1 of the addressed sector's header. Although the SC7000 Disk Controller can emulate both formats, all sectors contain 256 16-bit words in either format. If bit FER is set, then bit HCE may not be simultaneously set.

Massbus Parity Error (PAR) - Bit 03

This bit normally contains a zero unless a one is written to it.

Register Modification Refused (RMR) - Bit 02

This bit is set when a Write operation is attempted to any disk drive register, except registers RMMR1 or RMAS, while the DRY bit is reset. The operation in progress continues.

Illegal Register (ILR) - Bit 01

This bit is set when an attempt is made to address an illegal disk drive register. Only registers 0 to 15 are legal. The upper 16 registers are illegal.

Illegal Function (ILF) - Bit 00

This bit is set when an illegal function code (with GO set) is written into register RMCS1.

6.4.4 MAINTENANCE REGISTER 1 (RMMR1) **Base Address + 40C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

The Maintenance mode is not emulated. Writing to register RMMR1 can occur at any time, regardless of the status of the disk drive. A Drive Clear or Controller Clear command resets this register, except for bit 03, which is always set.

6.4.5 ATTENTION SUMMARY REGISTER (RMAS) **Base Address + 410**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

This register allows the program to examine the Attention status of all disk drives with only one register Read operation. It also provides a means of resetting the Attention Active logic in a selected group of disk drives. The eight low-order bits of this register correlate to the ATA bit in the disk drive that has the same logical disk drive unit number as the bit position in this register. The set condition of an ATA bit is logic one.

The ATA bit for a particular disk drive can be reset by loading a one into the bit position that correlates to the logical unit number of the disk drive. Loading a zero has no effect. For a program to use register RMAS without losing status information, it must use MOV instructions for all Write operations to this register. An instruction that does a Read-Restore function, such as BIS, may cause bits to be lost that were asserted just before the Read operation. The contents of this register can be read from or written to any any time. This register is replicated for every disk drive, and can be accessed with any disk drive address without causing NED errors. A persistent error, just like any error condition, causes the ATA bit to be reasserted. Attempts made to clear reasserted ATA bits are not successfully accomplished.

6.4.6 DISK ADDRESS REGISTER (RMDA) **Base Address + 414**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

This register is used to address the track and sector on the disk to or from which a Data Transfer operation is to be performed. The contents of register RMDA are incremented each time a sector of data is transferred so that consecutive sectors are automatically

addressed when the word count indicates that more than one sector of data is to be transferred. At the end of a Data Transfer operation, register RMDA contains the address of the sector which follows the last sector involved in a Data Transfer operation.

Register RMDA contains a sector counter that provides a count for up to 256 sectors/track. It also contains a track counter which is incremented by one every time the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to zero and the contents of register RMDC are incremented by one. The Invalid Address Error (IAE, RMER1 bit 10) is set if the address in register RMDA is not valid when a Data Transfer, Seek, or Search function is initiated. The maximum sector and track address are obtained from the selected configuration PROM.

6.4.7 DRIVE TYPE REGISTER (RMDT) **Base Address + 418**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit position always contains a one to indicate the disk drive is a moving-head device.

Dual-Port Mode (DPM) - Bit 11

This bit is set to signify the disk drive is operating in the Dual-Port mode when enabled by switch SW7-6 in the ON (CLOSED) position, or that it is operating in the Dual-Access mode when enabled by switch SW5-2 in the ON (CLOSED) position.

Drive Type Code - Bits <07:00>

This code specifies the type of disk drive, as listed in the following table:

Code	Disk Drive Type	Code	Disk Drive Type
14	RM03	16	RM80
15	RM02	17	RM05

6.4.8 LOOK-AHEAD REGISTER (RMLA) **Base Address + 41C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Sector Counter										0	0	0	0	0	0

This register contains the disk drive sector counter. It is used to present the angular position of the disk relative to the read/write heads for the addressed disk drive. Register RMLA provides the

programmer with a means of optimizing disk accesses by minimizing rotational delays. The sector counter typically counts from zero to the maximum sector count, or from zero to the maximum sector count minus two, depending on the status of the FMT16 bit (RMOF bit 12).

6.4.9 SERIAL NUMBER REGISTER (RMSN) **Base Address + 420**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW7 -8	SW7 -7	SW7 -6	SW7 -5	SW7 -4	SW7 -3	SW7 -2	SW7 -1	Firmware Revision						Port Number	

This register, for a DEC RM-type of disk drive, contains a four-decade serial number to distinguish that disk drive from similar disk drives attached to the SC7000 Disk Controller. The serial number consists of the states of option switches SW7-8 through SW7-1, the firmware revision level, and the port number to which the disk drive is attached.

6.4.10 OFFSET REGISTER (RMOF) **Base Address + 424**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	SSEI	0	OFD	0	0	0	0	0	0	0

This register contains three inhibit bits (ECI, HCI and SSEI), the Format Status (FMT16) bit, and the disk drive offset direction (OFD) bit. The status of bit OFD determines if a Read operation is to be done with the heads advanced or retarded from the normal track centerline position. The actual offset determination is done by the status of bit OFM (RMDS bit 00). All bits of this register are cleared by the Read-In Preset command.

Format Bit (FMT16) - Bit 12

This bit is set for 16-bit configuration and it is reset for 18-bit configuration. This bit position should always contain a one because the SC7000 Disk Controller only handles the 16-bits/word format. When this bit is set with an RM80 emulation, it operates with one less sector/track than the track contains. The extra sector is a skip sector that is used when a bad sector is detected. When this bit is set with an RM03 or RM05 emulation, the SC7000 Disk Controller operates with all of the configured sectors/track. In all applications, when this bit is reset, the SC7000 Disk Controller operates with two fewer sectors/track than the number of tracks for which the disk drive is configured. The status of this bit (and SSEI bit 09) affect the value of the maximum sector address that can be read from register RMHR (see subsection 6.4.12).

Error Correction Code Inhibit (ECI) - Bit 11

When this bit is set, it inhibits the automatic Error Correction procedure that would normally occur when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

When this bit is set, it inhibits Header Compare and CRC Check functions; therefore, the SC7000 Disk Controller depends only on the sector count for sector identification. Emulex recommends that this HCI bit be reset (cleared) during a Write operation.

Skip Sector Error Inhibit (SSEI) - Bit 09

This bit is used for RM80 emulations only, and is set to inhibit Skip Sector errors during a Header Check operation. When this bit is set, the disk drive operates on all sectors/track. This bit is reset whenever a Data Transfer command increments the contents of register RMDA to a new track address. This bit cannot be set unless the FMT16 bit is already set.

Offset Direction (OFD) - Bit 07

This bit is set via software control to select the direction of head positioner offset. The one status retards the heads, and the zero status advances the heads.

6.4.11 DESIRED CYLINDER REGISTER (RMDC) **Base Address + 428**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Desired Cylinder Address															

This register contains the address of the cylinder to which the head positioner, on the selected disk drive, is to move. It is cleared by the Read-In Preset command. After an initial Load operation, the value in this register is incremented by one whenever register RMDA is reset to zero during a Data Transfer operation. When the contents of register RMDC are incremented and the contents of register MBABCR do not equal zero, a Mid-Transfer Seek operation is initiated by the SC7000 Disk Controller.

When after asserting GO (RMCS1 bit 00), register RMDC contains an address greater than the largest addressable cylinder, IAE (RMER1 bit 10) is set.

6.4.12 HOLDING REGISTER (RMHR) **Base Address + 42C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a Read-only register, except for the following conditions:

a. If one of three values is written into this register, the configured capacity (size) of the addressed disk drive is read out as indicated in the following table:

value	Address
8017	Maximum cylinder address
8018	Maximum track address
8019	Maximum sector address (per RMOF contents)

b. Writing FFFF into this register enables the nonstandard Format command to be executed when that command is loaded into register RMCS1. The enable is cleared when any Data Transfer command terminates.

Whenever data is written into register RMDA, the complement of that data is placed in register RMHR.

6.4.13 MAINTENANCE REGISTER 2 (RMMR2) **Base Address + 430**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
13FF															

This Read-only register always returns 13FF when its contents are read.

6.4.14 ERROR REGISTER 2 (RMER2) **Base Address + 434**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

This Read/Write register contains status information that relates to the electromechanical performance of the addressed disk drive. Any set bit in this register causes ERR (RMDS bit 14) to be set. In some situations, UNS (RMER1 bit 14) is also set when a bit is set in this register. Writing zeros into this register should not be used as the normal method for clearing errors; a Drive Clear or Controller Clear command should be used instead. If the program attempts to write into this register while the disk drive is busy, RMR (RMER1 bit 02) is set and the Write command is ignored.

Bad Sector Error (BSE) - Bit 15

This bit is set whenever the SC7000 Disk Controller detects a zero in bit position 14 or 15 of the first header word while HCI (RMOF bit 10) equals zero.

Seek Incomplete (SKI) - Bit 14

This bit is set whenever a Seek Error signal is received from the addressed disk drive. Setting this bit also sets UNS (RMER1 bit 14). When the SC7000 Disk Controller detects a Seek Error, it automatically issues a Fault Clear command and a Return-To-Zero command to the addressed disk drive. The DRY bit (RMDS bit 07) is not set until the Return-To-Zero operation is completed.

Operator Plug Error (OPE) - Bit 13

This bit is set whenever the Address ID plug is removed from the selected disk drive and then reinstalled in that disk drive. It can be cleared by issuing a Drive Clear command. This error is usually caused when a disk drive momentarily fails to set its Select line on the B-Cable in response to its address on the A-Cable.

Invalid Command (IVC) - Bit 12

This bit is set whenever there exists one of the following conditions:

a. A command is issued to a disk drive while ERR (RMDS bit 14) is set or MOL (RMDS bit 12) is reset.

b. Any command except Read-In Preset, Pack Acknowledge, or NOP is issued to a disk drive while VV (RMDS bit 06) is reset.

Loss of Sector Clock (LSC) - Bit 11

This bit is set when the SC7000 Disk Controller detects more than 250 Sector pulses without an Index pulse (when Index and Sector pulses are on the B-Cable).

Loss of Bit Clock (LBC) - Bit 10

This bit is set if the SC7000 Disk Controller does not detect at least 16 Servo Clock pulses within 3.3 microseconds.

Multiple Drive Select (MDS) - Bit 09

This bit is set when more than one disk drive responds to a logical address on the A-Cable. This bit cannot be set by a programmed I/O Write operation.

DC Power Unsafe (DCU) - Bit 08

This bit is set if the -5 Vdc power supply to the cable drivers and receivers is not at the proper voltage level. This bit cannot be set by a programmed I/O Write operation.

Device Check (DVC) - Bit 07

This bit is set if a Fault status signal is received from the addressed disk drive. The set DVC bit causes UNS (RMER1 bit 14) to be set. When the SC7000 Disk Controller detects the Fault status indication, it automatically issues a Fault Clear command and a Return-To-Zero command. The ATA bit (RMDS bit 15) is set when the Return-To-Zero operation is completed.

AC Power Unsafe (ACU) - Bit 06

This bit is set if an ACLO Status signal is received from the bus. This bit cannot be set by a programmed I/O Write operation.

Skip Sector Error (SSE) - Bit 05

This bit is used for RM80 emulations only, and it is set whenever bit 13 of Header Word 1 is set while bit SSEI (RMOF bit 09) is reset. Setting this bit indicates the addressed sector has been skipped and the data is contained in the next sector. This bit cannot be written into unless the disk drive is an RM80 emulation.

Data Parity Error (DPE) - Bit 03

This bit position normally contains a zero unless it is written into.

6.4.15 ECC POSITION REGISTER (RMEC1) **Base Address + 438**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

This Read-only register contains the Error Correction Code (ECC) position of the error pattern, as determined by the ECC correction procedure. The ECC postion is the number of bit positions from the beginning of the data field in the addressed sector to (and including) the right-most bit position of the error pattern stored in register RMEC2 (see subsection 6.4.16). If the detected error cannot be corrected by using the ECC correction procedure, ECH (RMER1 bit 06) is set.

6.4.16 ECC PATTERN REGISTER (RMEC2) **Base Address + 43C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

This Read-only register contains the 11-bit error correction pattern obtained from the ECC correction procedure. A one in this error pattern indicates a bit of data in memory from the last-read sector is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement toward the right-most bit of the error correction pattern is determined by the bit count in register RMEC1 (see subsection 6.4.15). The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

6.4.17 ILLEGAL DISK DRIVE REGISTERS

The upper 16 disk drive registers (base address + 440 through base address + 47C) are illegal addresses. Attempts to access these locations sets ILR (RMER1 bit 01).

6.5 COMMANDS

Operations are initiated on the addressed disk drive by loading the function code and GO bit into register RMCS1. The function code specifies a specific command. The commands can be divided into five categories:

a. Data Transfer commands

b. Positioning commands

c. Housekeeping commands

d. Optional commands

e. Overlapped Seek and Search commands.

Commands and their corresponding function codes (always odd because the GO bit must be asserted to execute the command) are described in this subsection. Subsection titles for all commands in this subsection are followed by the function code in parenthesis.

6.5.1 DATA TRANSFER COMMANDS

These commands transfer data to or from the disk and are designated by function codes 29 through 3F.

All Data Transfer commands have Seek and Sector Search functions implied. When the desired cylinder does not equal the current cylinder during execution of a Data Transfer operation, a Seek to the desired cylinder is executed. The SC7000 Disk Controller then

searches the desired track for the desired sector and starts the Data Transfer operation when that desired sector has been found. If bit HCI (RMOF bit 10) is reset, then on all commands, except Header and Data commands, a match of the sector header must be made before the Data Transfer operation is started.

If bit HCI (RMOF bit 10) is set, the header is not compared or checked, and the command start point is based on the previously recorded Sector pulses, as is the command start point of the Write Header and Data command. With bit HCI set, header errors are not reported. With HCI cleared, the Data Transfer operation is aborted if a header error is detected. During execution of a Read/Write Check Header and Data command, only those sectors that follow the sector in which an error is detected are aborted.

The desired sector, track, and cylinder addresses are updated after the contents of each sector are transferred. Therefore, at the end of a Data Transfer operation, the disk is set up to transfer the contents of the next sequential sector. This event sequence arrangement allows multiple sectors of data to be transferred and it allows spiral transfers of data across tracks and cylinders. When the desired cylinder address changes during execution of a Data Transfer operation, an implied seek is performed, and in this circumstance, the implied seek is termed a Mid-Transfer Seek operation.

6.5.1.1 Write Check Data Command (29)

This command reads data from the selected disk drive and compares that data on a byte-by-byte basis with the data obtained from memory. If the data fails to compare, the WCU or WCL error status bit is set and the command is terminated immediately. For additional information about Write Check errors, see applicable bit descriptions in subsections 6.2, 6.3 and/or 6.4.

6.5.1.2 Write Check Header and Data Command (2B)

This command reads the contents of the header field and data field from the selected disk drive and compares it on a byte-by-byte basis with data obtained from memory. If the header or data fail to compare, the WCU or WCL error status bit is set and the command is terminated immediately.

6.5.1.3 Write Data Command (31)

This command writes the 512-byte data field of the selected sector with data obtained from memory. A two-word ECC is appended to each sector. After the data is transferred to a sector, the byte count is checked. If the byte count is not zero, the Data Transfer operation is continued to the next sector; otherwise the Write command is terminated. If the byte count goes to zero while a sector is being written, the rest of the sector is filled with zeros; then the Write Data command is terminated.

6.5.1.4 Write Header and Data Command (format) (33)

This command writes the four-byte header field and the 512-byte data field of the selected sector with data obtained from memory. A one-word Cyclic Redundancy Check Character (CRCC) is appended to each header field. After a sector of data is transferred, the byte count is checked. If the byte count is not zero, the Data Transfer operation is continued to the next sector; otherwise the Write Header and Data command is terminated. If the byte count goes to zero while a sector is being written, the rest of the sector is filled with zeros; then the Write Header and Data command is terminated.

6.5.1.5 Read Data Command (39)

This command reads the contents of the 512-byte data field from the selected sector and transfers that data to memory. When transfer of data from that sector is completed, the ECC is checked to verify that data read from the disk was error free. If a data error occurred and if bit ECI (RMOF bit 11) is reset, the ECC correction procedure is initiated to determine whether the error is or is not correctable. When the ECC correction procedure is done, the Read Data command is terminated to allow software to apply the correction information. If no data errors are detected by the ECC check, the byte count is checked. If the byte count is not zero, the Data Transfer operation is continued and the 512-byte data field from the next sector is read and transferred to memory. If the byte count goes to zero while the sector is being read, the rest of the sector is not transferred and the Read Data command is terminated.

6.5.1.6 Read Header and Data Command (3B)

This command reads the contents of the four-byte sector header field and the 512-byte data field from the selected sector and transfers that information to memory. When transfer of the data from that sector is completed, the ECC is checked to verify that data read from the disk was error free. If a data error occurred and if bit ECI (RMOF bit 11) is reset, the ECC correction procedure is initiated to determine whether the error is or is not correctable. When the ECC correction procedure is done, the Read Header and Data command is terminated to allow software to apply the correction information. If no data errors are detected by the ECC check, the byte count is checked. If the byte count is not zero, the Data Transfer operation is continued and the four-byte sector header field and the 512-byte data field from the next sector are read and transferred to memory. If the byte count goes to zero while the sector is being read, the rest of the sector is not transferred and the Read Header and Data command is terminated.

6.5.2 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack. They are completed in

milliseconds. When a positioning command is initiated, the SC7000 Disk Controller sets PIP and resets DRY (RMDS bits 13 and 07, respectively). When a positioning operation is completed, the SC7000 Disk Controller resets bits PIP and GO (RMDS bit 13, and RMCS1 bit 00, respectively), and sets bits DRY and ATA (RMDS bits 07 and 15, respectively, plus applicable ATA bit in RMAS).

6.5.2.1 Seek Command (05)

This command causes the heads to be moved to the cylinder address specified by the contents of register RMDC. When the SC7000 Disk Controller detects the Seek command with bit GO (RMCS1 bit 00) set, the cylinder address is sent to the corresponding disk drive. Any attempt to write into register RMDC while the Seek operation is in progress causes bit RMR (RMER1 bit 02) to be set and the contents of register RMDC are not modified. When the Seek operation is completed , bits ATA and DRY are set and bit GO is reset. If the disk drive is not able to complete the Seek command within 500 milliseconds or if it has moved the head carriage to a position beyond the recording field, the disk drive asserts the Seek Error signal and the SC7000 Disk Controller sets bit SKI (RMER2 bit 14) and bits ATA, ERR and DRY (RMDS bits 15, 14, and 07, respectively, plus applicable ATA bit in RMAS). The SC7000 Disk Controller has already issued a Fault Clear command and a Return-To-Zero command to the disk drive, so that a subsequent Drive Clear command can clear the error condition.

6.5.2.2 Recalibrate Command (07)

This command causes the disk drive positioner to position the heads over cylinder zero. A Return-To-Zero function is automatically performed with each Head Load sequence and whenever a Fault or Seek Error is detected. This command clears bit OFM (RMDS bit 00) if that bit was asserted.

6.5.2.3 Offset Command (0D)

This command sets bit OFM (RMDS bit 00). Subsequent Read operations are done with the heads offset from the track centerline in the direction specified by OFD (RMOF bit 07). The Offset operation allows additional data recovery attempts beyond the capability provided by the ECC correction procedure when an ECC error is detected. If an ECC hard error occurs, two offset positions should be tried. When the Offset command is completed, bit ATA is set to indicate a Read command should be issued to the cylinder and track for recovery of data.

Bit OFM in register RMDS is cleared by any of six methods:

a. Seek to another cylinder by means of Implied or Mid-Transfer Seek operation

b. Write command issued

c. Return-To-Centerline command issued

d. Recalibrate command issued

e. Read-In Preset command issued

f. Whenever disk drive cycles up from OFF state.

6.5.2.4 Return-To-Centerline Command (0F)

This command is used to clear bit OFM (RMDS bit 00) and set ATA bits (RMDS bit 15 and applicable bit in RMAS). It also resets bit OFD (RMOF bit 07).

6.5.2.5 Search Command (19)

The Search command causes the SC7000 Disk Controller to first perform a Seek operation to the desired cylinder and then compare the sector counter with the desired sector address in register RMDA. When they match, the SC7000 Disk Controller sets bits ATA, and if bit IE (MBACR bit 02) is set, an Interrupt is sent to the CPU. An unsuccessful completion of a Search command occurs when the comparison between the sector count and desired sector address is not made before the SC7000 Disk Controller has detected three Index pulses; bit OPI (RMER1 bit 13) is then set.

6.5.3 HOUSEKEEPING COMMANDS

The five housekeeping commands are used to place the disk drive logic into a known or initialized state; their execution usually requires a few microseconds.

6.5.3.1 No Op Command (01)

This command performs no operation, except to clear the ATA bits.

6.5.3.2 Drive Clear Command (09)

This command clears registers and conditions, associated with the selected disk drive, as specified in the following list: Bits ATA and ERR in register RMDS, applicable bit ATA in register RMAS, all contents of registers RMER1, RMER2, and RMEC2, and all bits in register RMMR1, except bit 03 which is set.

6.5.3.3 Release Command (08)

Unconditionally and in all modes, this command performs a Drive Clear function and then releases the addressed disk drive for use by the other port of the SC7000 Disk Controller.

6.5.3.4 Read-In Preset Command (11)

This command sets bit VV (RMDS bit 06). clears registers RMDC, RMDA and RMOF, and clears bit OFM (RMDS bit 00).

6.5.3.5 Pack Acknowledge Command (13)

This command sets bit VV (RMDS bit 06). If the selected disk drive has gone off line and then on line; i.e., state change of bit MOL (RMDS bit 12), this command, or a Read-In Preset command, must be issued before any Data Transfer command or Positioning command can be issued. The Pack Acknowledge command is primarily used to avoid unknown changes of the disk pack or removable cartridge.

6.5.4 NONSTANDARD COMMANDS

Only one nonstandard command is presently available for use by the SC7000 Disk Controller. The Format command can be executed only after writing FFFF into register RMHR.

6.5.4.1 Format Command (3F)

This command executes a Return-To-Zero function, clears registers RMDC and RMDA, and formats the entire disk pack in standard format. Each sector has bits 14, 15, and the FMT16 bit set in Header Word 1, and a data field that contains all zeros. When the Format command is done, register RMDC is set to contain the last cylinder number plus one, and bits LST (RMDS bit 10) and FMT16 (RMOF bit 12) are set. The Format command formats full tracks for all emulations. No Bad Sector File or Skip Sector File is written.

6.5.5 OVERLAPPED SEEK AND SEARCH COMMANDS

Normally, overlapped Seek commands and Search commands terminate and assert the ATA bits for the selected disk drive as soon as the disk drive heads are properly positioned. On systems with two logical disk drive units per physical disk drive, overlapped Seek commands or Search commands could be issued to both logical disk drive units on the same physical disk drive. In such a situation, handling is slightly different and the operations are governed by the following rules:

a. The first logical disk drive unit to be issued a Seek or Search command performs the physical Seek function and the other logical disk drive unit simulates the Seek function.

b. For Seek commands, the logical disk drive unit that performed the physical Seek operation asserts its ATA bits first. The other logical disk drive unit asserts its ATA bits about 45 microseconds later.

c. For Search commands, handling depends on the status of option switch SW7-4:

   1. If option switch SW7-4 is OFF (OPEN), the first logical disk drive unit that finds a rotational match after the physical Seek operation has ended asserts its ATA bits first.

   2. If option switch SW7-4 is ON (CLOSED), the logical disk drive unit that performed the physical Seek operation asserts its ATA bits first when a rotational match occurs after the physical Seek operation has ended. The other logical disk drive unit asserts its ATA bits **after** the first logical disk drive unit has asserted its ATA bits, and a rotational match subsequently occurs for the second logical disk drive unit. This event sequence allows the user to first service the logical disk drive unit which is actually on cylinder, and thus minimize physical Seek operations.

6.6 PROGRAMMING INFORMATION

This subsection provides explanations about programming techniques for Controller Clear, Error Clear and Drive Clear operations, for Interrupt conditions, for termination of Data Transfer operations and for Ready status indicators.

6.6.1 CONTROLLER CLEARING

The SC7000 Disk Controller can be cleared by using three different methods:

a. **Controller Clear** - The Controller Clear command is performed by writing a one-bit into the INIT bit position (MBACR bit 00), or by detecting a UBUS DCLO signal. The Controller Clear causes clearing or setting of the following registers and/or bits:

   - MBACR, MBASR, MBABCR, MBACSR <31:16>. Sets MBADR to BF.

   - In all disk drives: RMCS1 bits <06:00>; RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR, and LST bits; RMMR1 bits <15:04> and <02:00>. Sets bit 03 of RMMR1 and DRY (bit 07) of RMDS.

b. **Error Clear** - Error bits in register MBASR are cleared by writing a one-bit into the bit position or by the start of another valid Data Transfer operation.

c. **Drive Clear** - The Drive Clear command (function code 09) clears the following registers and/or bits in the addressed disk drive:

   o RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits <15:04> and <02:00>. Sets bit 03 of RMMR1.

6.6.2 INTERRUPT CONDITIONS

The SC7000 Disk Controller generates a CPU Interrupt if bit IE (MBACR bit 02) is set while there is present the following events or conditions:

a. Data Transfer operation terminates, either normally or abnormally.

b. Any disk drive Attention Active (ATA) bit is asserted.

c. There is asserted one or more of the following status bits:

Programming Error	(PGE)
Non-Existent Drive	(NED)
Missed Transfer Error	(MXE)
Power Down	(PDN)
Power Up	(PUP)

   The Power Up status condition automatically sets bit IE and generates an Interrupt to the CPU.

The Interrupt condition persists until the status bits that caused the Interrupt condition are cleared.

6.6.3 TERMINATION OF DATA TRANSFER OPERATIONS

A Data Transfer operation which has been successfully started may terminate in any of the following ways:

a. **Normal Termination** - Byte count overflows to zero and the SC7000 Disk Controller becomes Ready at the end of the current sector.

b. **Controller Error** - There is set in register MBASR one or more of the following bits:

Data Transfer Abort	(DTA)
Data Late	(DLT)
Write Check Upper Error	(WCU)
Write Check Lower Error	(WCL)
Missed Transfer Error	(MXE)
Exception	(EXC)
Invalid Map	(IM)
Error Confirmation	(EC)
Error Status	(ERS)
No Response Status	(NRS)
Interface Sequence Timeout	(ITO)
Read Data Timeout	(RTO)

c. **Drive Error** - The ERR bit in register RMDS and at least on bit in register RMER1 or register RMER2 is set. The ATA bit for the disk drive performing the Data Transfer operation becomes asserted.

d. **Program-Caused Abort** - The program can terminate a Data Transfer operation by setting the Abort (ABT) or Initialize (INIT) bits in register MBACR.

6.6.4 READY BITS

The Data Transfer Busy (DTB) bit in register MBASR is set when a Data Transfer operation is in progress. DTB is cleared when the Data Transfer operation is terminated. For Read operations, this termination occurs when the last word has been transferred to memory. For Write operations, this termination occurs when the last sector has been written. Data Transfer Complete (MBASR bit 13, DTC) is set when the Data Transfer operation terminates.

Drive Ready (RMDS bit 07, DRY) is the Ready indicator for the selected disk drive and is the complement of the disk drive GO bit (RMCS1 bit 00). To successfully initiate a Data Transfer command, the **DTB bit must be clear, and the DRY bit must be asserted,** but a command which does not involve transfer of data (Search, Drive Clear, etc.) may be issued to a disk drive at any time DRY is asserted regardless of the state of the DTB bit (MBASR bit 31).

When a Data Transfer command is initiated, DRY and DTC become negated and DTB becomes asserted.

6.6.5 DUAL-CONTROLLER OPERATION

SMD disk drives may be equipped with a Dual-Port option which allows two disk controllers (usually on separate computers) to access the same disk drive. The SC7000 Disk Controller supports this type of operation as a standard feature. The Dual-Port mode of operation for the SC7000 Disk Controller is selected by placing

switch SW7-6 in the ON (CLOSED) position. Most of the Dual-Port functions of the DEC controller being emulated are supported by the SC7000 Disk Controller; and those not supported should be transparent to a properly written Dual-Port driver software program. SC7000 Disk Controller register responses in Dual-Port mode of operation are summarized in Table 6-1.

6.6.5.1 Dual-Port Disk Drives

The two disk drive ports are designated Channel I and Channel II. Because only one SC7000 Disk Controller can access the disk drive at any time, access is granted on a first-come, first-served basis. Once an SC7000 Disk Controller has gained access to the disk drive, the other SC7000 Disk Controller is denied access until the operations being conducted by the first SC7000 Disk Controller have been completed. Each channel, however, has a physical switch which can be set to disable the other disk drive port and prevent the other associated SC7000 Disk Controller from having access to the disk drive.

6.6.5.2 Unseized State

The disk drive is in the Unseized state when it is not connected to either SC7000 Disk Controller. The CPU must issue a request for the SC7000 Disk Controller to seize the disk drive. This request is made by one of the following methods:

a. Writing into any disk drive register, including Read-only registers.

b. Writing a logic one into ATA bit position for the selected disk drive in register RMAS. The bit does not have to be set.

Table 6-1. Register Access on Dual Controller Operation

Disk Drive State	Response With Respect To Action On Channel I
Read Contents of RMCS1	
Disk Drive Not Seized	Reads all zeros. No request flag is set.
Disk Drive Seized by Channel I	DVA = 1; reads register contents; resets timer.
Disk Drive Seized by Channel II	DVA = 0; reads all zeros. No request flag is set

Table 6-1. Register access on Dual Controller Operation (continued)

Disk Drive State	Response With Respect To Action On Channel I
Read Contents of Any Other Disk Drive Register	
Disk Drive Not Seized	Reads all zeros.
Disk Drive Seized by Channel I	Reads register contents.
Disk Drive Seized by Channel II	Reads all zeros.
Write Into RMCS1	
Disk Drive Not Seized	Function code attempted if GO = 1 and a Port Request flag is set.
Disk Drive Seized by Channel I	Loads function code. (Switches to Unseized state if function code is a Release command.)
Disk Drive Seized by Channel II	Function code attempted if GO = 1 and a Port Request flag is set.
Write Into Any Disk Drive Register, Except RMCS1	
Disk Drive Not Seized	Write command ignored and a Port Request flag is set.
Disk Drive Seized by Channel I	Loads the register if not a Read-only register. Resets timer.
Disk Drive Seized by Channel II	Write command ignored and a Port Request flag is set.

6.6.5.3 Seized State

The disk drive is seized when it is logically connected to one of the SC7000 Disk Controllers. At that time, bit DVA (RMCS1, bit 11) is set to indicate the disk drive is ready to communicate with the SC7000 Disk Controller which has seized it. If the disk drive has already been seized by the other SC7000 Disk Controller, the DVA bit is not set, all the disk drive registers contain all zeros, and any attempt to write to a register in that SC7000 Disk Controller is ignored. Attempts to seize a disk drive which is busy with the

other port are remembered and acted on when the disk drive is released by the other SC7000 Disk Controller.

6.6.5.4 Returning to the Unseized State

The disk drive is released and returned to the Unseized state by issuing a Release command. The disk drive can also be released if a one-second timer in the SC7000 Disk Controller times out before one of the events, listed in subsection 6.6.5.2 for seizing the disk drive, is not performed periodically to keep resetting the timeout timer. Reading the contents of register RMCS1 also resets the timeout timer if the disk drive is currently seized. This reset allows the CPU to check the Seized/Unseized state of the selected disk drive, and if the disk drive is in the Seized state, the CPU need not be concerned about the occurrence of a time-out release.

When the SC7000 Disk Controller detects a previously busy disk drive becoming unseized, it examines the state of its Request flag. If the Request flag is set (access to the disk drive had been requested while the disk drive was busy on the other port), the SC7000 Disk Controller seizes the disk drive and sets the appropriate Attention Active (ATA) bit which causes an Interrupt request to be sent to the CPU if the Interrupt Enable (IE) bit is set. If the CPU does not respond to the Attention signal within one second, the disk drive is released, but the ATA bit remains set.

6.6.5.5 DEC Compatibility

The SC7000 Disk Controller differs from the equivalent DEC controller in three important aspects:

a. **No Neutral State.** Limitations of the daisy-chained A-Cable and the microprocessor organization of the SC7000 Disk Controller do not allow instantaneous access to all disk drives at the same time; therefore the SC7000 Disk Controller assumes the disk drive is busy on the other port if the SC7000 Disk Controller has not already seized that disk drive. Reading the contents of register RMCS1 always indicates the disk drive is seized by the other SC7000 Disk Controller (bit DVA, RMCS1 bit 11 equals zero) unless the disk drive has been previously requested. The CPU must request the disk drive by writing into any drive register and waiting until the appropriate ATA bit is set. The set ATA bit indicates the SC7000 Disk Controller has seized the disk drive. If the disk drive was actually not seized by the other SC7000 Disk Controller, the ATA bit is set almost immediately. DEC controllers, however, can switch from Neutral to Seized state within the time required to do a single Read or Write operation to/from a disk drive register. Therefore, if the selected disk drive is not already seized, no ATA bit is set and the disk drive is immediately available to the seizing controller.

b. **Noninstantaneous Release Command.** Release command execution is not instantaneous because the SC7000 Disk Controller needs a few microseconds for command execution. During this time interval, the selected disk drive appears to be in the Unseized state.

c. **No Poll.** During a Data Transfer operation, the timeout timers do not operate and the disk drives cannot be polled to determine if they are or are not busy. Therefore, no disk drives are seized or released during execution of a Data Transfer operation.

The software driver should not issue a Release command and then attempt to save the current status of a disk drive, because the Release command immediately shows the disk drive in the Unseized state, thus returning zero data for the contents of the disk drive registers. To allow the other SC7000 Disk Controller time to poll the selected disk drive, the CPU should not communicate with any of the disk drive registers for the released disk drive until it is required to again seize the disk drive.

6.6.5.6 Dual-Port Disk Drives in Single-Port Mode

When using an operating system which does not have dual-port disk drive software support, it may still be advantageous to use dual-port disk drives while operating the SC7000 Disk Controller in the Single-Port mode. This operating condition allows for a nondynamic method of operation between two CPU systems. In this type of operation, the SC7000 Disk Controller does not logically unseize (release) the disk drive, and in effect, the disk drive is seized by both controllers in the system all the time.

The one-second timer (and the Release command) operate exactly as described in subsection 6.6.5.5. Even when released, a disk drive still appears to the releasing controller as a seized disk drive. No Attention signal is generated when the other controller finds the disk drive not busy. If a command is issued to a controller while a disk drive is busy on the other port, that controller must wait until the disk drive becomes not busy before executing the command. The SC7000 Disk Controller waits indefinitely for the disk drive to become unbusy.

This Single-Port mode of operation eliminates the need for manually switching the disk drive from one SC7000 Disk Controller to another.

6.6.5.7 Dual-Access Mode

The SC7000 Disk Controller provides compatibility with the VAX/VMS system, when that system is configured for dual-access operation, when DIP switch SW5-2 is placed in the ON (CLOSED) position. When the SC7000 Disk Controller is in the Dual-Access mode, it sets the

Dual-Port mode (DPM) bit in register RMDT and the Programmable (PGM) bit in register RMDS to imitate the DEC Neutral state. The SC7000 Disk Controller still functions in Single-Port mode as described in subsection 6.6.5.6.

When bits DPM and PGM are set, the operating system attempts to seize a disk drive by simply writing a command to it. If the disk drive is not busy, the command is executed. If the disk drive is already busy on its other port, the SC7000 Disk Controller waits until that disk drive is released and then seizes and commands that disk drive. The VAX/VMS system has a timer with a sufficiently long period to prevent causing a Timeout event when the SC7000 Disk Controller is forced to wait.

The first time the SC7000 Disk Controller detects a disk drive, that disk drive is ignored for one second. This one-second stall occurs once for each disk drive on the SC7000 Disk Controller. The stall prevents the SC7000 Disk Controller from detecting erroneous status information when power is applied to the disk drive after the SC7000 Disk Controller has been powered up. For a disk drive in the Dual-Port mode, the stall prevents the other CPU from accessing the disk drive until the Stall function is completed. The Dual-Access option switch bypasses the Stall function in all applications. For proper system operation with the Dual-Access option switch in the ON position, all disk drives must have power applied before either SC7000 Disk Controller in the system is powered up.

Setting the Dual-Port option switch in the ON (CLOSED) position overrides the Dual-Access option, except for the power-up stall.

7.1 OVERVIEW

This section describes the architectural organization of the SC7000 Disk Controller and the format for disk organization. This section is divided into three subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	Architectural Organization
7.3	Disk Format

7.2 ARCHITECTURAL ORGANIZATION

A block diagram of the major functional elements of the V-MASTER/780 organization is shown in Figure 7-1. It shows the relationship of the Bus Translator and Bus Interface PCBAs to the SC7000 Disk Controller. Detailed block diagrams of the SC7000 Disk Controller itself, when used in the VAX-11/750 CPU and in the V-MASTER VAX-11/780 CPU are shown in Figures 7-2 and 7-3, respectively.

7.2.1 V-MASTER/780

The V-MASTER/780 requires two additional PCBAs to complete the subsystem. If the SC7000 Disk Controller is intended for use in a VAX-11/750 CPU system, these PCBAs are not required.

7.2.1.1 Bus Interface

The Bus Interface PCBA (Emulex P/N SU7810401) provides the conventional interface with the SBI of the VAX-11/780 CPU. It includes circuitry for six functions.

a. Bus transceivers

b. Parity generation and checking

c. Address tag and identification (ID) decoding

d. Sequence status logic

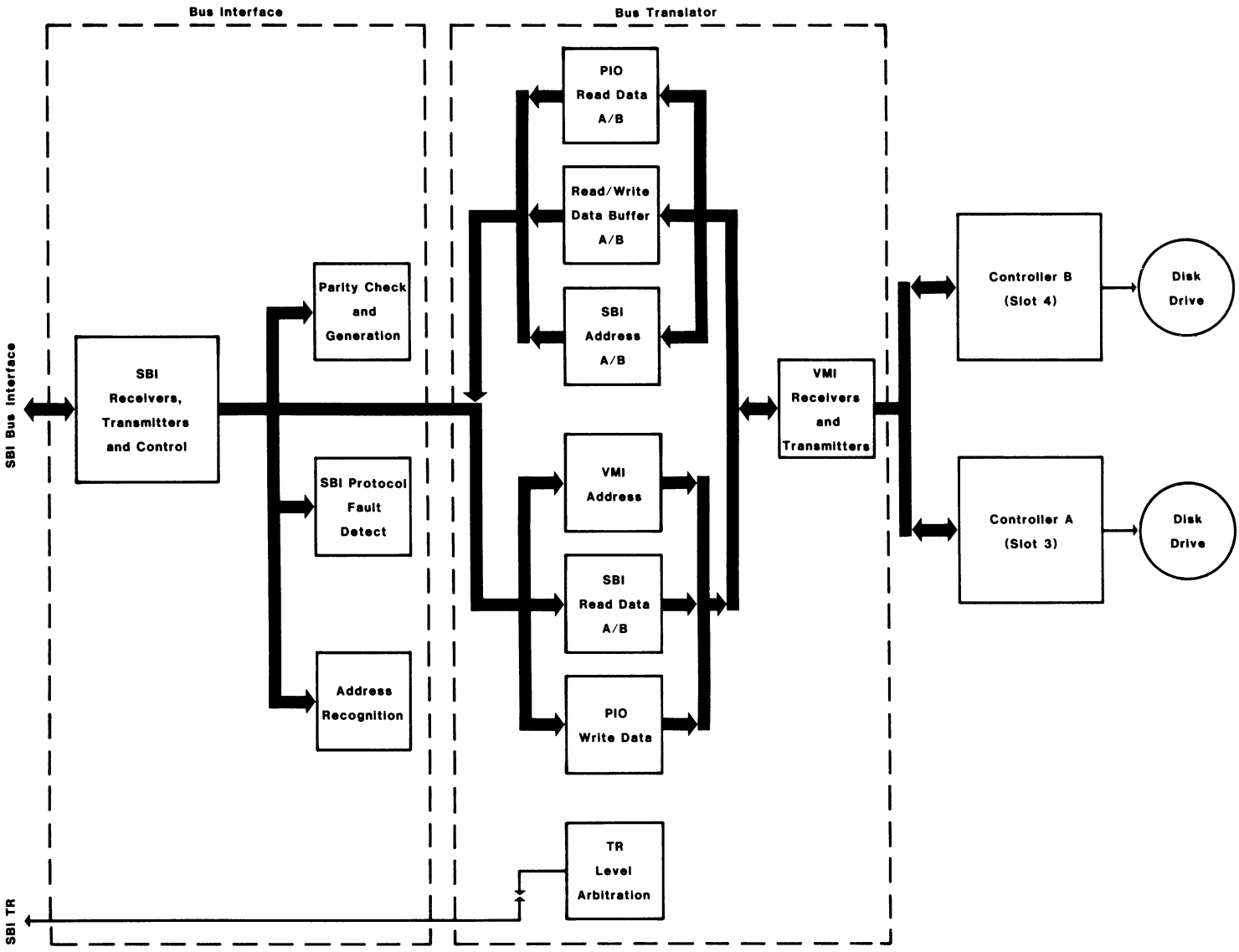


Figure 7-1. V-MASTER Block Diagram

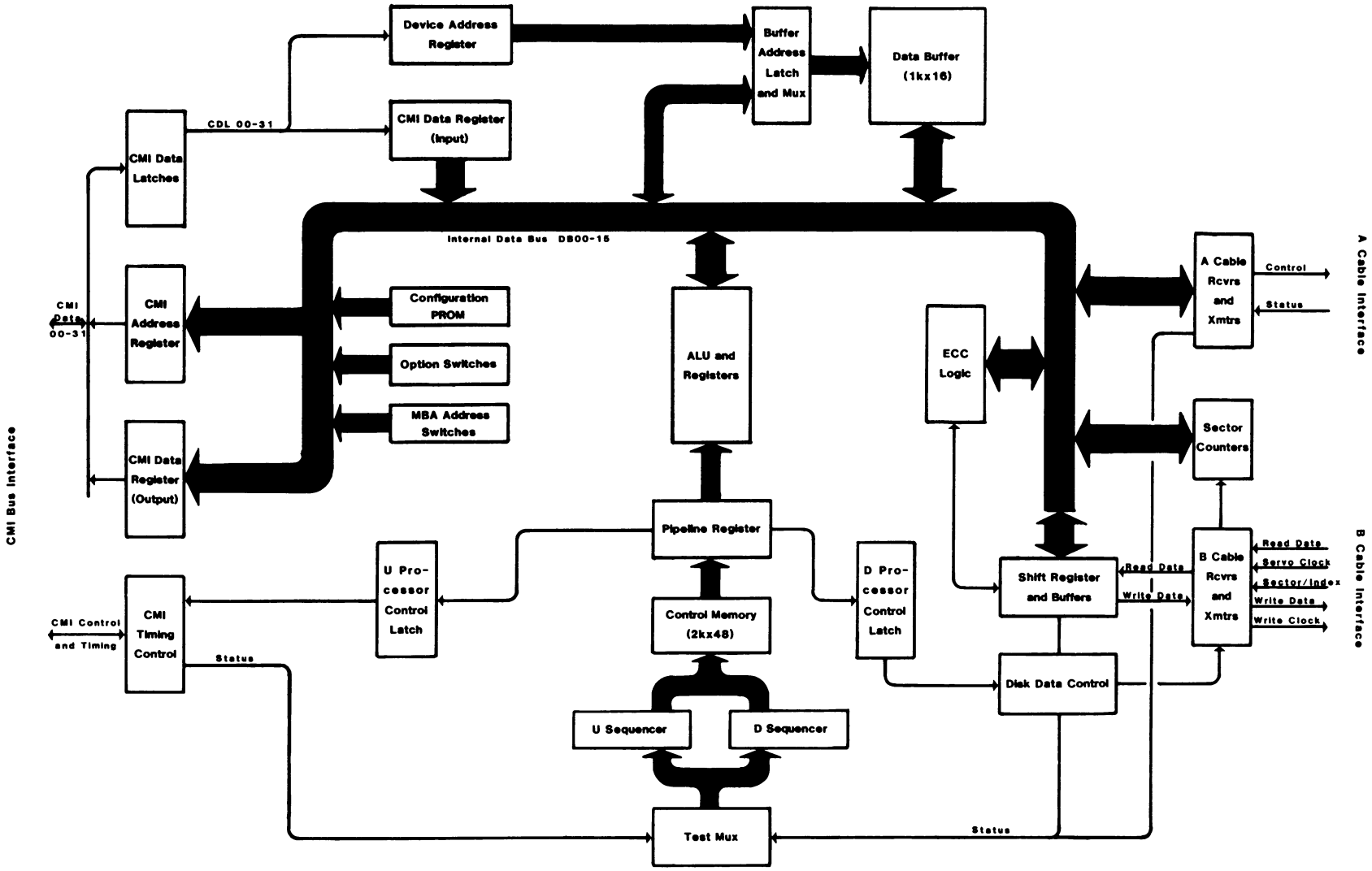


Figure 7-2. SC7000 Disk Controller in VAX-11/750 CPU, Block Diagram

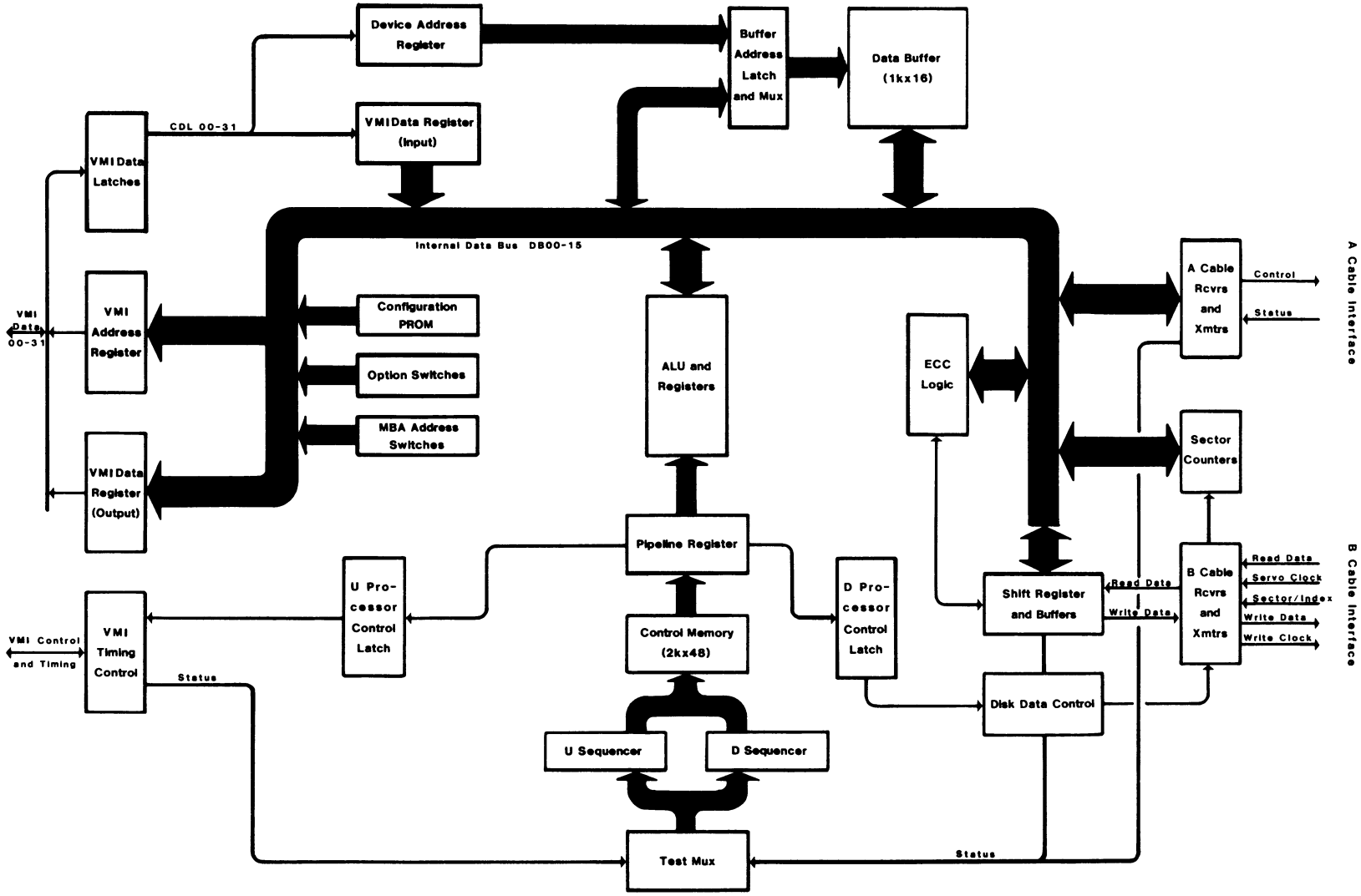


Figure 7-3. SC7000 Disk Controller in VAX-11/780 CPU, Block Diagram

e. Interface and Read Data timeouts

f. SBI fault detection.

7.2.1.2 Bus Translator

The Bus Translator PCBA (Emulex P/N SU7810402) provides signal translation between the SBI output from the Bus Interface PCBA and the SC7000 Disk Controller PCBA (Emulex P/N SU7510410). The SC7000 Disk Controller PCBA interfaces with the Bus Translator PCBA via the V-MASTER Interface (VMI) bus. The VMI bus permits two SC7000 Disk Controllers to be used as part of the V-MASTER/780. The Bus Translator PCBA provides the SBI arbitration logic, storage for programmed I/O address and data, and storage of direct memory access (DMA) addresses and data. Its primary function is to buffer between the longword DMA on the SBI and the quadword transfer to the VMI. When doing disk Write operations, memory data words are automatically prefetched and transferred to the buffers on the Bus Transfer PCBA to enable more efficient operation of the VMI bus. The Bus Translator PCBA provides DMA buffering capability for two SC7000 Disk Controllers. The SC7000 Disk Controller requires a Bus Translator PCBA of revision level D or later.

7.2.1.3 SC7000 Disk Controller

The SC7000 Disk Controller is organized around a 16-bit, high-speed bipolar microprocessor. The arithmetic logic unit (ALU) and register file portion of the microprocessor are implemented with four AMD 2901 bit-slice components. The microinstruction is 48 bits long, and the control memory of 4K words is implemented with six 4K x 8-bits programmable Read-only memory (PROM) integrated circuits (ICs) that can be plugged into IC sockets on the SC7000 Disk Controller PCBA.

The SC7000 Disk Controller contains a 4K x 16-bit high-speed random access memory (RAM) buffer which temporarily stores the contents of the MBA registers, Disk Drive registers, and Map registers, plus 12 sectors of data.

The A-Cable register (ACR) provides storage for all A-Cable signals going to the disk drives. The A-Cable inputs from the selected disk drive are testable by the microprocessor.

Serial data from the selected disk drive is converted into 16-bit parallel data and transferred to the RAM buffer via the microprocessor. Parallel data accessed from the RAM buffer by the microprocessor is serialized and sent to the selected disk drive under control of the Servo Clock pulse received from the disk drive.

A 32-bit error correction code (ECC) shift register generates and checks the ECC for the data field in each sector of data. This register is also used in a 16-bit Cyclic Redundancy Check Character (CRCC) mode for the sector headers. The actual ECC polynomial operation is done independently of the microprocessor, but

determination of the error position and error pattern is controlled by the microprocessor.

A configuration PROM is a source to the data bus. This PROM configures the maximum cylinder address, maximum track address, maximum sector address, and the disk drive type code for each logical disk drive unit in the system.

In the VAX-11/750 CPU system, the CMI bus is 32 bits wide. It transfers addresses and programmed I/O and DMA data. The microprocessor responds to all programmed I/O and does functions required for the addressed controller register. The microprocessor controls all DMA operations and transfers between the CMI bus and the internal RAM buffer.

In the V-MASTER VAX-11/780 CPU system, the VMI bus is 32 bits wide and is used for programmed I/O and Data Transfer operations. It transfers addresses and data. DMA operations transfer 32-bit dualwords to the V-MASTER/780, which does 64-bit quadword transfers to the SBI bus. The microprocessor responds to all programmed I/O and does functions required for the addressed controller register. The microprocessor controls all DMA operations and transfers data between the VMI bus and the internal RAM buffer.

7.3 DISK FORMAT

This subsection describes the general organizational format of the disks, track and cylinder meaning, sector organization and header details.

7.3.1 DISK ORGANIZATION

The SC7000 Disk Controller emulates one or two logical RM-type disk drive units per each physical disk drive attached to the SMD interface. The Unit Select number of the physical disk drive must be in the range from zero to three unless option switch SW7-2 is ON (see Appendix A).

When a physical disk drive has two logical RM-type disk drive units mapped upon it, the first logical disk drive unit is mapped onto the first half of the heads (tracks) and has a logical disk drive unit number that is the same as the Unit Select number of the physical disk drive. The second logical disk drive unit is mapped upon the second half of the heads (tracks) and has a logical disk drive unit number that is four greater than the Unit Select number of the physical disk drive. For instance, four physical disk drives could each have two logical disk drive units mapped on them which would have logical disk drive unit numbers zero through three, and four through seven, and the CPU would be working with eight logical disk drive units, even through only four physical disk drives were connected in the system.

7.3.2 TRACK AND CYLINDER MAPPING

When the number of heads (tracks) on the physical disk drive is equal to the number of tracks on the RM-type disk drive that is being emulated, a one-to-one correspondence between tracks and cylinders exists. This correspondence is essential for media-compatible disk packs such as RM03 and RM05. When the physical disk drive has a number of heads which is different than the RM-type disk drive configuration, the SC7000 Disk Controller operates in a Mapped Track and Cylinder mode.

7.3.3 SECTOR ORGANIZATION

Figure 7-4 shows the sector format used by the SC7000 Disk Controller in media-compatible mode. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four-byte header is preceded by a preamble of 30 bytes which ends in the synchronization (sync) byte and which is followed by a two-byte CRCC. The 256-word data field is preceded by a preamble of 20 bytes which ends in a sync byte and which is followed by four bytes of the ECC. This format is compatible with that of the DEC RM02/RM03 and RM05 disk drives.

If the actual amount of useful data information is less than 512 bytes, the remainder of the data field is filled with zeros until 512 bytes have been written. During disk formatting procedures, each data track is located and recorded with header information by using the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual sectors or groups of sectors should not be reformatted unless absolutely necessary.

7.3.4 HEADER

Figure 7-5 shows the header format, which consists of the following three words:

Word One -

This word contains the cylinder address in bits <11:00>. It also contains a logic one in bit position 12 to identify the 16-bit format to the software and logic one in bit positions 14 and 15 to identify a good sector. For RM80 disk drive emulations, a logic one in bit position 13 (SSF) indicates the data for this sector has been relocated to the next sector.

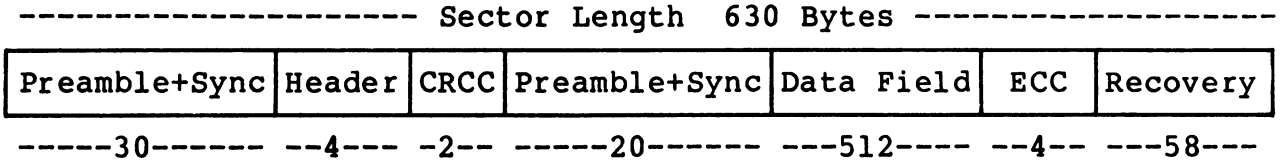


Figure 7-4. Sector Format

Header Word 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	SSF	1	Cylinder Address											

Header Word 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Track Address								Sector Address							

Header Word 3

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Cyclic Redundancy Check Character (CRCC) Code															

Figure 7-5. Header Format

Word Two -

The low-order eight bits of this word contain the sector address. The upper byte of this word contains the track (head) address.

Word Three -

This word contains the Cyclic Redundancy Check Character (CRCC) code which is generated and checked by the logic in the SC7000 Disk Controller. This word is not available to the software.

7.3.4.1 Header Field Handling

After the disk drive reports it is on the addressed cylinder, the SC7000 Disk Controller locates the desired sector by means of sector counters maintained in its circuitry. A sector counter is maintained for each physical disk drive unit. The SC7000 Disk Controller compares the first two words of the header with the, desired (addressed) cylinder, track and sector, and then checks the CRCC word for errors. An error in the header field is indicated by asserting the appropriate error status bit in the error register (format error, header compare error, bad sector error, skip sector error or CRCC error). A header error is only valid when the sector count field of register RMLA and the sector field of register RMDA have already matched. It is immaterial where a CRCC error occurs in the header field because the SC7000 Disk Controller cannot determine the location of the CRCC error in the header field; however, software may read the header to memory by using the Read Header and

Data command. The header compare may be inhibited by setting bit 10 (HCI) in register RMOF.

BLANK

8.1 OVERVIEW

This section lists pin/signal assignments for the CPU and disk drive interfaces, and is divided into six subsections as listed in the following table:

Subsection	Title
8.1	Overview
8.2	Disk Drive SMD Interface
8.3	Controller CMI/VMI Interface
8.4	V-MASTER/780 SBI Pin/Signals
8.5	Bus Interface PCBA Pin/Signals
8.6	Bus Translator PCBA Pin/Signals

8.2 DISK DRIVE SMD INTERFACE

The disk drive SMD interface consists of a 60-conductor A-Cable and a 26-conductor B-Cable. At the Cable Paddleboard PCBA, the A-Cable is split to mate with a 34-pin connector and a 26-pin connector. At the disk drive end of the A-Cable, all 60 conductors are attached to a single 60-pin connector.

Table 8-1 lists SMD interface pin/signal assignments for A-Cable connector J1 on the Cable Paddleboard PCBA.

NOTE

In the From/To columns of pin/signal tables in this section, 'To' means the driving circuit is in the SC7000 Disk Controller and 'From' means the driving circuit is in the disk drive. In the L/H columns of pin/signal tables in this section, 'L' means the low level is the true state of the signal and 'H' means the high level is the true state of the signal. Symbols '+' and '-' indicate polarity of the differential signal level; i.e., when the + line is driven 0.2 Volt more positive than the - line, the signal level is being driven true.

Table 8-1. Pin/Signal Assignments, A-Cable Connector J1

Pin	±	Signal Name	(Tag 3 Function)	±	Pin	From/To
1	-	Tag 1		+	18	To
2	-	Tag 2		+	19	To
3	-	Tag 3		+	20	To
4	-	Bit 0	(Write Gate)	+	21	To
5	-	Bit 1	(Read Gate)	+	22	To
6	-	Bit 2	(Servo Offset Plus)	+	23	To
7	-	Bit 3	(Servo Offset Minus)	+	24	To
8	-	Bit 4	(Fault Clear)	+	25	To
9	-	Bit 5	(AM Enable)	+	26	To
10	-	Bit 6	(Return To Zero)	+	27	To
11	-	Bit 7	(Data Strobe Early)	+	28	To
12	-	Bit 8	(Data Strobe Late)	+	29	To
13	-	Bit 9	(Release)	+	30	To
14	-	Open Cable Detect		+	31	To
15	+	Fault		-	32	From
16	-	Seek Error		+	33	From
17	-	On Cylinder		+	34	To

Table 8-2 lists SMD interface pin/signal assignments for A-Cable connector J2 on the Cable Paddleboard PCBA.

Table 8-2. Pin/Signal Assignments, A-Cable Connector J2

Pin	±	Signal Name	±	Pin	From/To
1	+	Bit 10 High	-	14	To
2		Power Sequence Hold/Pick*		15	To
3	+	Write Protect	-	16	From
4	+	Unit Select Bit 3	-	17	To
5	+	Unit Select Bit 2	-	18	To
6	-	Sector	+	19	From
7	+	Unit Select Bit 1	-	20	To
8	+	Unit Select Bit 0	-	21	To
9	+	Unit Select Tag	-	22	To
10	+	Busy (Dual-Port Only)	-	23	From
11	-	Address Mark Found	+	24	From
12	-	Unit Ready	+	25	From
13	-	Index	+	26	From

* Pin 2 (+) and pin 15 (-) = Hold
Pin 2 (-) and pin 15 (+) = Pick

Table 8-3 lists SMD interface pin/signal assignments for the 60-pin connector at the disk drive end of the A-Cable.

Table 8-3. Pin/Signal Assignments, A-Cable 60-Pin Connector

Pin	±	Signal Name	(Tag 3 Function)	±	Pin	From/To
1	-	Tag 1		+	31	To
2	-	Tag 2		+	32	To
3	-	Tag 3		+	33	To
4	-	Bit 0	(Write Gate)	+	34	To
5	-	Bit 1	(Read Gate)	+	35	To
6	-	Bit 2	(Servo Offset Plus)	+	36	To
7	-	Bit 3	(Servo offset Minus)	+	37	To
8	-	Bit 4	(Fault Clear)	+	38	To
9	-	Bit 5	(AM Enable)	+	39	To
10	-	Bit 6	(Return To Zero)	+	40	To
11	-	Bit 7	(Data Strobe Early)	+	41	To
12	-	Bit 8	(Data Strobe Late)	+	42	To
13	-	Bit 9	(Release)	+	43	To
14	-	Open Cable Detect		+	44	To
15	-	Fault		+	45	From
16	-	Seek Error		+	46	From
17	-	On Cylinder		+	47	From
18	-	Index		+	48	From
19	-	Unit Ready		+	49	From
20	-	Address Mark Found		+	50	From
21	-	Busy (Dual-Port Only)		+	51	From
22	-	Unit Select Tag		+	52	To
23	-	Unit Select Bit 0		+	53	To
24	-	Unit Select Bit 1		+	54	To
25	-	Sector		+	55	From
26	-	Unit Select Bit 2		+	56	To
27	-	Unit Select Bit 1		+	57	To
28	-	Write Protected		+	58	From
29		Power Sequence Hold/Pick*			59	To
30	-	Bit 10		+	60	To

* Pin 29 (+) and pin 59 (-) = Hold
Pin 29 (-) and pin 59 (+) = Pick

8.3 CONTROLLER CMI/VMI INTERFACE

Table 8-4 lists pin/signal assignments for the SC7000 Disk Controller PCBA edge connectors. In this table, CMI (as used for VAX-11/750 CPU systems) is same as VMI (as used for V-MASTER VAX-11/780 CPU systems. Similarly, signal 780 ST in V-MASTER VAX-11/780 CPU system would be 750 ST in VAX-11/750 CPU system.

Table 8-4. Pin/Signal Assignments, SC7000 Disk Controller PCBA

Side 1	Connector A			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
NOT USED		1	2		NOT USED
NOT USED		3	4		NOT USED
NOT USED		5	6		NOT USED
NOT USED		7	8		NOT USED
PRESENT	L	9	10		NOT USED
NOT USED		11	12		NOT USED
NOT USED		13	14		NOT USED
NOT USED		15	16		NOT USED
NOT USED		17	18		NOT USED
NOT USED		19	20		+5V
NOT USED		21	22		NOT USED
0V		23	24		0V
NOT USED		25	26		NOT USED
NOT USED		27	28		NOT USED
NOT USED		29	30		NOT USED
NOT USED		31	32		NOT USED
NOT USED		33	34		NOT USED
NOT USED		35	36		NOT USED
NOT USED		37	38		+5V
NOT USED		39	40		NOT USED
DMA EN	H	41	42	H	CLR
NOT USED		43	44		NOT USED
NOT USED		45	46		NOT USED
NOT USED		47	48	L	780 ST
DMA READ	H	49	50	L	DMA SEI
NOT USED		51	52		NOT USED
NOT USED		53	54		NOT USED
NOT USED		55	56	L	MBA SEL 0
NOT USED		57	58		+5V
NOT USED		59	60		NOT USED
NOT USED		61	62		NOT USED
NOT USED		63	64		NOT USED
NOT USED		65	66		NOT USED
BG4 IN	H	67	68	H	BG4 OUT
BG5 IN	H	69	70	H	BG5 OUT
0V		71	72		0V
BG6 IN	H	73	74	H	BG6 OUT
NOT USED		75	76		NOT USED
BG7 IN	H	77	78	H	BG7 OUT
NOT USED		79	80	L	BUS BR5
NOT USED		81	82		NOT USED
NOT USED		83	84	L	CMI ARB 1
CMI ARB 2	L	85	86	L	CMI ARB 3
CMI ARB 4	L	87	88	L	CMI ARB 5
CMI ARB 6	L	89	90	L	CMI ARB 7
-15V		91	92	L	CMI HOLD
CMI WAIT	L	93	94		NOT USED

Table 8-4. Pin/Signal Assignments, SC7000 Disk Controller PCBA (continued)

Side 1	Connector B			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
CMI DATA 00	H	1	2		NOT USED
CMI DATA 01	H	3	4	H	CMI DATA 02
CMI DATA 03	H	5	6	H	CMI DATA 04
CMI DATA 05	H	7	8	H	CMI DATA 06
CMI DATA 07	H	9	10	H	CMI DATA 08
NOT USED		11	12	H	CMI DATA 09
CMI DATA 10	H	13	14	H	CMI DATA 11
CMI DATA 12	H	15	16	H	CMI DATA 13
CMI DATA 14	H	17	18	H	CMI DATA 15
CMI DATA 16	H	19	20		+5V
CMI DATA 17	H	21	22	H	CMI DATA 18
0V		23	24		NOT USED
CMI DATA 19	H	25	26	H	CMI DATA 20
CMI DATA 21	H	27	28	H	CMI DATA 22
NOT USED		29	30	H	CMI DATA 23
CMI DATA 24	H	31	32	H	CMI DATA 25
CMI DATA 26	H	33	34	H	CMI DATA 27
CMI DATA 28	H	35	36	H	CMI DATA 29
CMI DATA 30	H	37	38		+5V
CMI DATA 31	H	39	40	L	CMI STATUS 00
CMI STATUS 01	L	41	42	L	CMI DBBZ
0V		43	44		0V
CMI B CLK	L	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50		NOT USED
NOT USED		51	52		NOT USED
0V		53	54	H	TAG 2
TAG 1	H	55	56	H	US 1
US 2	H	57	58	H	US 0
US TAG	H	59	60	H	BIT 9
BIT 8	H	61	62	H	BIT 10
TAG 5	H	63	64	H	BIT 6
BIT 7	H	65	66	H	BIT 5
BIT 4	H	67	68	H	BIT 1
BIT 0	H	69	70	H	BIT 2
BIT 3	H	71	72		+ WRITE PROT
- WRITE PROT		73	74		+ SEEK ERROR
- SEEK ERROR		75	76		- ON CYLINDER
+ ON CYLINDER		77	78		+ BUSY
- BUSY		79	80		- SECTOR
+ SECTOR		81	82		- UNIT READY
+ UNIT READY		83	84		+ INDEX
- INDEX		85	86		- FAULT
+ 5V		87	88		+ FAULT
- 5V		89	90	L	PCK HLD
- 5V		91	92		0V
NOT USED		93	94		NOT USED

Table 8-4. Pin/Signal Assignments, SC7000 Disk Controller PCBA (continued)

Side 1	Connector C			Side 2
Signal	L/H	Pin	Pin L/H	Signal
NOT USED		1	2	NOT USED
NOT USED		3	4	NOT USED
+ SEEK END 0		5	6	- SEEK END 0
- READ CLOCK 0		7	8	+ READ CLOCK 0
+ READ DATA 0		9	10	- READ DATA 0
- SERVO CLOCK 0		11	12	+ SERVO CLOCK 0
+ WRITE CLOCK 0		13	14	- WRITE CLOCK 0
- WRITE DATA 0		15	16	+ WRITE DATA 0
+ WRITE DATA 1		17	18	- WRITE DATA 1
- WRITE CLOCK 1		19	20	+ WRITE CLOCK 1
- SEEK END 1		21	22	+ SEEK END 1
+ READ CLOCK 1		23	24	- READ CLOCK 1
- READ DATA 1		25	26	+ READ DATA 1
+ SERVO CLOCK 1		27	28	- SERVO CLOCK 1
+ INDEX 0		29	30	- INDEX 0
- SECTOR 0		31	32	+ SECTOR 0
+ INDEX 1		33	34	- INDEX 1
- SECTOR 1		35	36	+ SECTOR 1
- SELECTED 1		37	38	+ SELECTED 1
+ SELECTED 0		39	40	- SELECTED 0
NOT USED		41	42	0V
NOT USED		43	44	0V
UBUS ACLO	L	45	46	+5V
NOT USED		47	48	NOT USED
NOT USED		49	50	NOT USED
0V		51	52	0V
0V		53	54	0V
+ SELECTED 3		55	56	- SELECTED 3
- SELECTED 2		57	58	+ SELECTED 2
- SECTOR 3		59	60	+ SECTOR 3
+ INDEX 3		61	62	- INDEX 3
- SECTOR 2		63	64	+ SECTOR 2
+ INDEX 2		65	66	- INDEX 2
+ SEEK END 2		67	68	- SEEK END 2
- READ CLOCK 2		69	70	+ READ CLOCK 2
+ READ DATA 2		71	72	- READ DATA 2
- SERVO CLOCK 2		73	74	+ SERVO CLOCK 2
- WRITE CLOCK 2		75	76	+ WRITE CLOCK 2
+ WRITE DATA 2		77	78	- WRITE DATA 2
- WRITE DATA 3		79	80	+ WRITE DATA 3
+ WRITE CLOCK 3		81	82	- WRITE CLOCK 3
+ SEEK END 3		83	84	- SEEK END 3
- READ CLOCK 3		85	86	+ READ CLOCK 3
- READ DATA 3		87	88	+ READ DATA 3
- SERVO CLOCK 3		89	90	+ SERVO CLOCK 3
NOT USED		91	92	0V
UBUS DCLO	L	93	94	NOT USED

8.4 V-MASTER/780 SBI PIN SIGNALS

Table 8-5 lists pin/signal assignments for the 12 SBI connectors.

Table 8-5. Pin/Signal Assignments, SBI Connectors

Connector	Pin	L/H	Signal Name	Pin	Connector
J1	A		GROUND	B	J7
J1	B	L	BUS SBI B00	A	J7
J1	C		GROUND	D	J7
J1	D	L	BUS SBI B01	C	J7
J1	E		GROUND	F	J7
J1	F		GROUND	E	J7
J1	H		GROUND	J	J7
J1	J	L	BUS SBI B02	H	J7
J1	K		GROUND	L	J7
J1	L		GROUND	K	J7
J1	M		(NOT USED)	N	J7
J1	N		(NOT USED)	M	J7
J1	P		GROUND	R	J7
J1	R	L	BUS SBI B03	P	J7
J1	S		GROUND	T	J7
J1	T		GROUND	S	J7
J1	U		GROUND	V	J7
J1	V		GROUND	U	J7
J1	W		GROUND	X	J7
J1	X		GROUND	W	J7
J1	Y		GROUND	Z	J7
J1	Z		GROUND	Y	J7
J1	AA		GROUND	BB	J7
J1	BB	L	BUS SBI B04	AA	J7
J1	CC		GROUND	DD	J7
J1	DD	L	BUS SBI B07	CC	J7
J1	EE		GROUND	FF	J7
J1	FF	L	BUS SBI B05	EE	J7
J1	HH		GROUND	JJ	J7
J1	JJ		GROUND	HH	J7
J1	KK		GROUND	LL	J7
J1	LL	L	BUS SBI B08	KK	J7
J1	MM		GROUND	NN	J7
J1	NN	L	BUS SBI B06	MM	J7
J1	PP		GROUND	RR	J7
J1	RR	L	BUS SBI 09	PP	J7
J1	SS		GROUND	TT	J7
J1	TT	L	BUS SBI B10	SS	J7
J1	UU		GROUND	VV	J7
J1	VV	L	BUS SBI B11	UU	J7

Table 8-5. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J2	A		GROUND	B	J8
J2	B		(NOT USED)	A	J8
J2	C		GROUND	D	J8
J2	D		(NOT USED)	C	J8
J2	E		GROUND	F	J8
J2	F		GROUND	E	J8
J2	H		GROUND	J	J8
J2	J		GROUND	H	J8
J2	K		GROUND	L	J8
J2	L	L	BUS SBI B12	K	J8
J2	M		GROUND	N	J8
J2	N	L	BUS SBI B14	M	J8
J2	P		GROUND	R	J8
J2	R		GROUND	P	J8
J2	S		GROUND	T	J8
J2	T	L	BUS SBI B13	S	J8
J2	U		GROUND	V	J8
J2	V		GROUND	U	J8
J2	W		GROUND	X	J8
J2	X	L	BUS SBI B15	W	J8
J2	Y		GROUND	Z	J8
J2	Z		GROUND	Y	J8
J2	AA		GROUND	BB	J8
J2	BB		GROUND	AA	J8
J2	CC		GROUND	DD	J8
J2	DD		GROUND	CC	J8
J2	EE		GROUND	FF	J8
J2	FF		GROUND	EE	J8
J2	HH		GROUND	JJ	J8
J2	JJ	L	BUS SBI B16	HH	J8
J2	KK		GROUND	LL	J8
J2	LL		GROUND	KK	J8
J2	MM		GROUND	NN	J8
J2	NN		GROUND	MM	J8
J2	PP		GROUND	RR	J8
J2	RR	L	BUS SBI B17	PP	J8
J2	SS		GROUND	TT	J8
J2	TT	L	BUS SBI B18	SS	J8
J2	UU		GROUND	VV	J8
J2	VV	L	BUS SBI B19	UU	J8

Table 8-5. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J3	A		GROUND	B	J9
J3	B		GROUND	A	J9
J3	C		GROUND	D	J9
J3	D	L	BUS SBI B20	C	J9
J3	E		GROUND	F	J9
J3	F	L	BUS SBI B23	E	J9
J3	H		GROUND	J	J9
J3	J	L	BUS SBI B21	H	J9
J3	K		GROUND	L	J9
J3	L		GROUND	K	J9
J3	M		GROUND	N	J9
J3	N	L	BUS SBI B22	M	J9
J3	P		GROUND	R	J9
J3	R		GROUND	P	J9
J3	S		GROUND	T	J9
J3	T		GROUND	S	J9
J3	U		GROUND	V	J9
J3	V		GROUND	U	J9
J3	W		GROUND	X	J9
J3	X		GROUND	W	J9
J3	Y		GROUND	Z	J9
J3	Z		GROUND	Y	J9
J3	AA		GROUND	BB	J9
J3	BB	L	BUS SBI B24	AA	J9
J3	CC		GROUND	DD	J9
J3	DD	L	BUS SBI B27	CC	J9
J3	EE		GROUND	FF	J9
J3	FF	L	BUS SBI B25	EE	J9
J3	HH		GROUND	JJ	J9
J3	JJ	L	BUS SBI B28	HH	J9
J3	KK		GROUND	LL	J9
J3	LL	L	BUS SBI B26	KK	J9
J3	MM		GROUND	NN	J9
J3	NN	L	BUS SBI B29	MM	J9
J3	PP		GROUND	RR	J9
J3	RR	L	BUS SBI B30	PP	J9
J3	SS		GROUND	TT	J9
J3	TT	L	BUS SBI FAIL	SS	J9
J3	UU		GROUND	VV	J9
J3	VV	L	BUS SBI B31	UU	J9

Table 8-5. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J4	A		GROUND	B	J10
J4	B	L	BUS SBI M0	A	J10
J4	C		GROUND	D	J10
J4	D	L	BUS SBI DEAD	C	J10
J4	E		GROUND	F	J10
J4	F	L	BUS SBI M1	E	J10
J4	H		GROUND	J	J10
J4	J	L	BUS SBI M3	H	J10
J4	K		GROUND	L	J10
J4	L	L	BUS SBI M2	K	J10
J4	M		GROUND	N	J10
J4	N	L	BUS SBI P0	M	J10
J4	P		GROUND	R	J10
J4	R	L	BUS SBI SPARE 0	P	J10
J4	S		GROUND	T	J10
J4	T	L	BUS SBI P1	S	J10
J4	U		GROUND	V	J10
J4	V		GROUND	U	J10
J4	W		GROUND	X	J10
J4	X		GROUND	W	J10
J4	Y		GROUND	Z	J10
J4	Z	L	BUS SBI SPARE 1	Y	J10
J4	AA		GROUND	BB	J10
J4	BB	L	BUS SBI TAG 0	AA	J10
J4	CC		GROUND	DD	J10
J4	DD	L	BUS SBI ID0	CC	J10
J4	EE		GROUND	FF	J10
J4	FF	L	BUS SBI TAG 1	EE	J10
J4	HH		GROUND	JJ	J10
J4	JJ		GROUND	HH	J10
J4	KK		GROUND	LL	J10
J4	LL	L	BUS SBI ID1	KK	J10
J4	MM		GROUND	NN	J10
J4	NN	L	BUS SBI TAG 2	MM	J10
J4	PP		GROUND	RR	J10
J4	RR	L	BUS SBI ID2	PP	J10
J4	SS		GROUND	TT	J10
J4	TT	L	BUS SBI ID3	SS	J10
J4	UU		GROUND	VV	J10
J4	VV	L	BUS SBI ID4	UU	J10

Table 8-5. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J5	A		GROUND	B	J11
J5	B	L	BUS SBI REQ 4	A	J11
J5	C		GROUND	D	J11
J5	D	L	BUS SBI REQ 7	C	J11
J5	E		GROUND	F	J11
J5	F	L	BUS SBI REQ 5	E	J11
J5	H		GROUND	J	J11
J5	J	L	BUS SBI TP	H	J11
J5	K		GROUND	L	J11
J5	L		GROUND	K	J11
J5	M		GROUND	N	J11
J5	N	L	BUS SBI REQ 6	M	J11
J5	P		GROUND	R	J11
J5	R	H	BUS SBI P CLK	P	J11
J5	S		GROUND	T	J11
J5	T	H	BUS SBI TP	S	J11
J5	U		GROUND	V	J11
J5	V		GROUND	U	J11
J5	W		GROUND	X	J11
J5	X	H	BUS SBI PD CLK	W	J11
J5	Y		GROUND	Z	J11
J5	Z	L	BUS SBI P CLK	Y	J11
J5	AA		GROUND	BB	J11
J5	BB	L	BUS SBI PD CLK	AA	J11
J5	CC		GROUND	DD	J11
J5	DD	L	BUS SBI MP2	CC	J11
J5	EE		GROUND	FF	J11
J5	FF	L	BUS SBI MP1	EE	J11
J5	HH		GROUND	JJ	J11
J5	JJ		GROUND	HH	J11
J5	KK		GROUND	LL	J11
J5	LL	L	SBI BUS ALERT	KK	J11
J5	MM		GROUND	NN	J11
J5	NN	L	SBI BUS UNJAM	MM	J11
J5	PP		GROUND	RR	J11
J5	RR	L	BUS SBI CNF 0	PP	J11
J5	SS		GROUND	TT	J11
J5	TT	L	BUS SBI FAULT	SS	J11
J5	UU		GROUND	VV	J11
J5	VV	L	BUS SBI CNF 1	UU	J11

Table 8-5. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J6	A		GROUND	B	J12
J6	B	L	BUS SBI INTLK	A	J12
J6	C		GROUND	D	J12
J6	D	L	BUS SBI TR01	C	J12
J6	E		GROUND	F	J12
J6	F	L	BUS SBI TR00	E	J12
J6	H		GROUND	J	J12
J6	J	L	BUS SBI TR03	H	J12
J6	K		GROUND	L	J12
J6	L	L	BUS SBI TR02	K	J12
J6	M		GROUND	N	J12
J6	N	L	BUS SBI TR04	M	J12
J6	P		GROUND	R	J12
J6	R		GROUND	P	J12
J6	S		GROUND	T	J12
J6	T	L	BUS SBI TR05	S	J12
J6	U		GROUND	V	J12
J6	V	L	BUS SBI TR06	U	J12
J6	W		GROUND	X	J12
J6	X	L	BUS SBI TR07	W	J12
J6	Y		GROUND	Z	J12
J6	Z	L	BUS SBI TR08	Y	J12
J6	AA		GROUND	BB	J12
J6	BB		GROUND	AA	J12
J6	CC		GROUND	DD	J12
J6	DD	L	BUS SBI TR09	CC	J12
J6	EE		GROUND	FF	J12
J6	FF	L	BUS SBI TR10	EE	J12
J6	HH		GROUND	JJ	J12
J6	JJ	L	BUS SBI TR11	HH	J12
J6	KK		GROUND	LL	J12
J6	LL	L	BUS SBI TR13	KK	J12
J6	MM		GROUND	NN	J12
J6	NN		GROUND	MM	J12
J6	PP		GROUND	RR	J12
J6	RR	L	BUS SBI TR12	PP	J12
J6	SS		GROUND	TT	J12
J6	TT	L	BUS SBI TR14	SS	J12
J6	UU		GROUND	VV	J12
J6	VV	L	BUS SBI TR15	UU	J12

8.5 BUS INTERFACE PCBA PIN/SIGNALS

Table 8-6 lists pin/signal assignments for the Bus Interface PCBA edge connectors.

NOTE

Edge connectors on all plug-in PCBAs have odd-numbered pins on the component side (side 1) and even-numbered pins on the solder side (side 2).

Table 8-6. Pin/Signal Assignments, Bus Interface PCBA

Side 1	Connector A			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
INTERRUPT ODD	H	1	2	H	INTERRUPT EVEN
TWO CHANNEL	L	3	4	L	BUS SBI B00
NOT USED		5	6	L	BUS SBI B01
NOT USED		7	8		NOT USED
NOT USED		9	10	L	BUS SBI B02
NOT USED		11	12		NOT USED
BUS MBA INT B00	H	13	14		NOT USED
NOT USED		15	16	L	BUS SBI B03
BUS MBA INT B01	H	17	18	H	BUS MBA INT B02
BUS MBA INT B03	H	19	20		+5V
BUS MBA INT B04	H	21	22	H	BUS MBA INT B05
GND		23	24		GND
BUS MBA INT B06	H	25	26	L	BUS SBI B04
BUS MBA INT B07	H	27	28	L	BUS SBI B07
HOLD TR	H	29	30	L	BUS SBI B05
SEND TR	H	31	32	L	BUS SBI B08
SEND TR HOLD	H	33	34	L	BUS SBI B06
BUS MBA INT B08	H	35	36	L	BUS SBI B09
BUS MBA INT B09	H	37	38		+5V
NOT USED		39	40	L	BUS SBI B10
NOT USED		41	42	L	BUS SBI B11
GND		43	44		GND
BUS MBA INT B10	H	45	46	H	BUS MBA INT B11
NOT USED		47	48		NOT USED
NOT USED		49	50		NOT USED
GND		51	52		GND
TS0	L	53	54		NOT USED
NOT USED		55	56		NOT USED
NOT USED		57	58		+5V
BUS MBA INT B12	H	59	60	H	BUS MBA INT B13
BUS MBA INT B14	H	61	62	H	BUS MBA INT B15
TR SEL A	H	63	64	L	BUS SBI B12
TR SEL B	H	65	66	L	BUS SBI B14
TR SEL C	H	67	68		NOT USED
NOT USED		69	70	L	BUS SBI B13
GND		71	72		GND

Table 8-6. Pin/Signal Assignments, Bus Interface PCBA (continued)

Side 1	Connector A			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
NOT USED		73	74	L	BUS SBI B15
NOT USED		75	76		+5V
BUS MBA INT B16	H	77	78	H	BUS MBA INT B17
NOT USED		79	80		NOT USED
BUS MBA INT B18	H	81	82	H	BUS MBA INT B19
BUS MBA INT B20	H	83	84		NOT USED
NOT USED		85	86	L	BUS SBI B16
TR SEL D	H	87	88		NOT USED
NOT USED		89	90	L	BUS SBI B17
BUS MBA INT B21	H	91	92	L	BUS SBI B18
BUS MBA INT B22	H	93	94	L	BUS SBI B19
Side 1	Connector B			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
NOT USED		1	2	H	BUS MBA INT B23
NOT USED		3	4	L	BUS SBI B20
NOT USED		5	6	L	BUS SBI B23
NOT USED		7	8	L	BUS SBI B21
NOT USED		9	10		NOT USED
NOT USED		11	12	L	BUS SBI B22
NOT USED		13	14		NOT USED
NOT USED		15	16		NOT USED
NOT USED		17	18		NOT USED
GEN MAP PAR	H	19	20		+5V
NOT USED		21	22	L	BUS SBI B24
GND		23	24		GND
NOT USED		25	26	L	BUS SBI B27
PGM INIT	L	27	28	L	BUS SBI B25
PWRF INIT	L	29	30	L	BUS SBI B28
NOT USED		31	32	L	BUS SBI B26
SET PGE	L	33	34	L	BUS SBI B29
NOT USED		35	36	L	BUS SBI B30
NOT USED		37	38		+5V
NOT USED		39	40	L	BUS SBI B31
CLK EXT CMD	H	41	42		NOT USED
GND		43	44		GND
CLK EXT READ	H	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50	H	BUS MBA INT B24
GND		51	52		GND
BUS MBA INT B25	H	53	54	H	BUS MBA INT B26
BUS MBA INT B27	H	55	56	H	BUS MBA INT B28
BUS MBA INT B29	H	57	58	H	BUS MBA INT B30
BUS MBA INT B31	H	59	60	L	BUS SBI M0
WRITE FCN	H	61	62	L	BUS SBI M1

Table 8-6. Pin/Signal Assignments, Bus Interface PCBA (continued)

Side		Connector B			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
NOT USED		63	64	L	BUS SBI M3
NOT USED		65	66	L	BUS SBI M2
NOT USED		67	68	L	BUS SBI P0
NOT USED		69	70		NOT USED
GND		71	72		GND
RMW FCN	H	73	74	L	BUS SBI P1
EXP WD	H	75	76	H	EX OP DONE
CLK VALID CMD	H	77	78	L	BUS SBI TAG 0
REC FAULT	L	79	80	H	BUS SBI ID0
NOT USED		81	82	L	BUS SBI TAG 1
NOT USED		83	84	L	BUS SBI ID1
STORED SBI B11	H	85	86	L	BUS SBI TAG 2
+5V		87	88	L	BUS SBI ID2
SET 1S TIMEOUT	L	89	90	L	BUS SBI ID3
SET RD TIMEOUT B	L	91	92	L	BUS SBI ID4
SET RD TIMEOUT A	L	93	94	L	WRITE DATA
Side 1		Connector C			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
ARB OK	L	1	2	L	BUS SBI REQ 4
NOT USED		3	4	L	BUS SBI REQ 7
UNEXP RD FLT	H	5	6	L	BUS SBI REQ 5
INTERRUPT CPU	L	7	8	L	BUS SBI TP
MULTI XMIT FLT	H	9	10	H	ID0 STORED
WRITE SEQ FLT	H	11	12	L	BUS SBI REQ 6
XMITTED FLT	H	13	14	H	BUS SBI PCLK
RD ADR	H	15	16	H	BUS SBI TP
DT READ	H	17	18	H	INT RD REQ
NOT USED		19	20	H	BUS SBI PDCLK
CMD REQ	L	21	22	L	BUS SBI PCLK
GND		23	24		GND
PARITY FLT	H	25	26	L	BUS SBI PDCLK
SET CORRECT RD	L	27	28	H	CLK DIB 2
CLK DIB 1	H	29	30	L	SET RD SUB
ENAB WDE MUX	H	31	32	L	SET CMD READY
NOT USED		33	34	L	BUS SBI UNJAM
INIT COND	L	35	36	L	BUS SBI CONF0
NOT USED		37	38	L	BUS SBI FAULT
INT DIF T1 CLK	L	39	40	L	BUS SBI CONF1
UNJAM	L	41	42	H	INT BUS 0 CLK
GND		43	44		GND
NOT USED		45	46		+5V
INT DIF T1 CLK	L	47	48	L	RD PEND A
INT DIF T3 CLK	L	49	50	H	INT DIF T3 CLK

Table 8-6. Pin/Signal Assignments, Bus Interface PCBA (continued)

Side 1	Connector C			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
GND		51	52		GND
INT BUS 1 CLK	L	53	54	L	CHNL ADR
INT DIF T0 CLK	L	55	56	H	INT DIF T0 CLK
INT DIF T2 CLK	H	57	58		NOT USED
INT DIF T2 CLK	L	59	60		NOT USED
BYTE MASK 1-0	H	61	62		NOT USED
BYTE MASK 1-2	H	63	64		NOT USED
BYTE MASK 1-1	H	65	66		NOT USED
NOT USED		67	68		NOT USED
BYTE MASK 1-3	H	69	70		NOT USED
GND		71	72		GND
DT GO	L	73	74	H	BYTE MASK 2-2
BYTE MASK 2-3	H	75	76	H	BYTE MASK 2-1
BYTE MASK 2-0	H	77	78		NOT USED
-5.2V		79	80	H	STROBE MAP
NOT USED		81	82		-5.2V
NOT USED		83	84		NOT USED
SET ERROR CNF	L	85	86	L	REQ COMPLETE
SET N/R CNF	L	87	88		NOT USED
+5V PS DCLO	H	89	90	H	-5V PS DCLO
+5V PS ACLO	H	91	92	H	-5V PS ACLO
WD2 ACK	H	93	94	H	ENAB WD1 MUX

8.6 BUS TRANSLATOR PCBA PIN/SIGNALS

Table 8-7 lists pin/signal assignments for the Bus Translator PCBA edge connectors.

Table 8-7. Pin/Signal Assignments, Bus Translator PCBA

Side 1	Connector A			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
INTERRUPT ODD	H	1	2	H	INTERRUPT EVEN
TWO CHNL	L	3	4		NOT USED
NOT USED		5	6		NOT USED
NOT USED		7	8		NOT USED
B PRESENT	L	9	10	L	A PRESENT
NOT USED		11	12		NOT USED
BUS MBA INT B00	H	13	14		NOT USED
NOT USED		15	16		NOT USED
BUS MBA INT B01	H	17	18	H	BUS MBA INT B02
BUS MBA INT B03	H	19	20		+5V
BUS MBA INT B04	H	21	22	H	BUS MBA INT B05

Table 8-7. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1	Connector A			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
GND		23	24		GND
BUS MBA INT B06	H	25	26		NOT USED
BUS MBA INT B07	H	27	28		NOT USED
HOLD TR	H	29	30		NOT USED'
SEND TR	H	31	32		NOT USED
SEND TR HOLD	H	33	34		NOT USED
BUS MBA INT B08	H	35	36		NOT USED
BUS MBA INT B09	H	37	38		+5V
CLR B	H	39	40	H	CLR A
DMA EN B	H	41	42	H	DMA EN A
GND		43	44		GND
BUS MBA INT B10	H	45	46	H	BUS MBA INT B11
780 ST B	L	47	48	L	780 ST A
DMA READ B	H	49	50	H	DMA READ A
GND		51	52		GND
DMA SEL B	L	53	54		NOT USED
MBA SEL 0 B	L	55	56	L	MBA SEL 0 A
NOT USED		57	58		+5V
BUS MBA INT B12	H	59	60	H	BUS MBA INT B13
BUS MBA INT B14	H	61	62		NOT USED
TR SEL A	H	63	64		NOT USED
TR SEL B	H	65	66		NOT USED
TR SEL C	H	67	68		NOT USED
BG5 IN B	H	69	70	H	BG5 IN A
GND		71	72		GND
NOT USED		73	74		NOT USED
NOT USED		75	76		+5V
BUS MBA INT B16	H	77	78	H	BUS MBA INT B17
BUS BR5 B	L	79	80	L	BUS BR5 A
BUS MBA INT B18	H	81	82	H	BUS MBA INT B19
BUS MBA INT B20	H	83	84	L	ARB 1
ARB 2	L	85	86	L	ARB 3
ARB 4	L	87	88	L	ARB 5
ARB 6	L	89	90	L	ARB 7
BUS MBA INT B21	H	91	92	L	CMI HOLD
BUS MBA INT B22	H	93	94		NOT USED

Side 1	Connector B			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
CMI DATA B00	H	1	2	H	BUS MBA INT B23
CMI DATA B01	H	3	4	H	CMI DATA B02
CMI DATA B03	H	5	6	H	CMI DATA B04
CMI DATA B05	H	7	8	H	CMI DATA B06
CMI DATA B07	H	9	10	H	CMI DATA B08
NOT USED		11	12	H	CMI DATA B09

Table 8-7. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1	Connector B			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
CMI DATA B10	H	13	14	H	CMI DATA B11
CMI DATA B12	H	15	16	H	CMI DATA B13
CMI DATA B14	H	17	18	H	CMI DATA B15
CMI DATA B16	H	19	20		+5V
CMI DATA B17	H	21	22	H	CMI DATA B18
GND		23	24		NOT USED
CMI DATA B19	H	25	26	H	CMI DATA B20
CMI DATA B21	H	27	28	H	CMI DATA B22
PWRF INIT	L	29	30	H	CMI DATA B23
CMI DATA B24	H	31	32	H	CMI DATA B25
CMI DATA B26	H	33	34	H	CMI DATA B27
CMI DATA B28	H	35	36	H	CMI DATA B29
CMI DATA B30	H	37	38		+5V
CMI DATA B31	H	39	40	L	CMI STATUS 00
CMI STATUS 01	L	41	42	L	CMI DBB2
GND		43	44		GND
CMI B CLK	L	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50	H	BUS MBA INT B24
GND		51	52		GND
BUS MBA INT B25	H	53	54	H	BUS MBA INT B26
BUS MBA INT B27	H	55	56	H	BUS MBA INT B28
BUS MBA INT B29	H	57	58	H	BUS MBA INT B30
BUS MBA INT B31	H	59	60	L	BUS SBI DEAD
WRITE FCN	H	61	62		NOT USED
NOT USED		63	64		NOT USED
NOT USED		65	66		NOT USED
NOT USED		67	68		NOT USED
NOT USED		69	70		NOT USED
GND		71	72		GND
NOT USED		73	74		NOT USED
EXP WD	H	75	76	H	EXT OP DONE + T0
CLK VALID CMD	H	77	78		NOT USED
REC FAULT	L	79	80		NOT USED
NOT USED		81	82		NOT USED
NOT USED		83	84		NOT USED
STORED SBI B11	H	85	86		NOT USED
+5V		87	88		NOT USED
SET 1S TIMEOUT	L	89	90		NOT USED
SET RD TIMEOUT B	L	91	92		NOT USED
SET RD TIMEOUT A	L	93	94		NOT USED

Table 8-7. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1	Connector C			Side 2
Signal	L/H	Pin	Pin	L/H	Signal
ARB OK	L	1	2		NOT USED
NOT USED		3	4		NOT USED
UNEXP RD FLT	H	5	6		NOT USED
INTERRUPT CPU	L	7	8		NOT USED
MULTI XMIT FLT	H	9	10	H	ID0 STORED
WRITE SEQ FLT	H	11	12		NOT USED
XMITTED FLT	H	13	14		NOT USED
RD ADR	H	15	16		NOT USED
DT READ	H	17	18		NOT USED
NOT USED		19	20		NOT USED
CMD REG	L	21	22		NOT USED
GND		23	24		GND
PARITY FLT	H	25	26		NOT USED
SET CORRECT RD	L	27	28	H	CLK DIB 2
CLK DTB 1	H	29	30	L	SET RD SUB
ENAB WDE MUX	H	31	32	L	SET CMD READY
NOT USED		33	34		NOT USED
INIT COND	L	35	36		NOT USED
NOT USED		37	38		NOT USED
INT DIF T1 CLK	L	39	40		NOT USED
UNJAM	L	41	42	H	INT BUS 0 CLK
GND		43	44		GND
UBUS ALCO	L	45	46		+5V
INT DIF T1 CLK	H	47	48		NOT USED
INT DIF T3 CLK	L	49	50	H	INT DIF T3 CLK
GND		51	52		GND
INT BUS CLK	L	53	54	L	CHNL ADR
INT DIF T0 CLK	L	55	56	H	INT DIF T0 CLK
INT DIF T2 CLK	H	57	58	L	BUS SBI TR01
INT DIF T2 CLK	L	59	60	L	BUS SBI TR00
BYTE MASK 1-0	H	61	62	L	BUS SBI TR03
BYTE MASK 1-2	H	63	64	L	BUS SBI TR02
BYTE MASK 1-1	H	65	66	L	BUS SBI TR04
NOT USED		67	68	L	BUS SBI TR05
BYTE MASK 1-3	H	69	70	L	BUS SBI TR06
GND		71	72		GND
BYTE MASK 2-2	H	73	74	L	BUS SBI TR07
BYTE MASK 2-3	H	75	76	L	BUS SBI TR08
BYTE MASK 2-0	H	77	78	H	BYTE MASK 2-1
-5.2V		79	80	L	BUS SBI TR09
NOT USED		81	82	L	BUS SBI TR10
NOT USED		83	84	L	BUS SBI TR11
SET ERROR CNF	L	85	86	L	REQ COMPLETE
SET N/R CNF	L	87	88		NOT USED
+5V PS DCLO	H	89	90	H	-5V PS DCLO
+5V PS ACLO	H	91	92	H	-5V PS ACLO
UBUS DLCO	L	93	94	H	ENAB WD1 MUX

BLANK

Appendix A
SC7000/B1 CONFIGURATION AND OPTION SELECTION

A.1 OVERVIEW

The SC7000 Disk Controller supports a wide variety of disk drive types and offers a number of other user-selectable options. This appendix is intended as a quick reference to help the user select disk drives and configure the SC7000 Disk controller for optimum utility. This appendix is divided into four subsections, as listed in the following table:

Subsection	Title
A.1	Overview
A.2	Controller Configuration
A.3	SC7000/B1 User-Selectable Options
A.4	Bus Interface PCBA Option Switches

A.2 CONTROLLER CONFIGURATION

The SC7000/B1 Disk Controller can control a wide variety of disk drives of various capacities (sizes) and types. The various disk drives that are supported are defined by the Configuration PROM. Table A-1 lists and defines the disk drive types and capacities supported by the SC7000/B1 Disk Controller. The user may select available options by means of configuration switches SW1, SW2, SW3, and SW4, which correlate to physical disk drive numbers 0, 1, 2, and 3, respectively. Correct switch settings for each of the various configurations are listed and described in Table A-2.

A.2.1 PHYSICAL VERSUS LOGICAL DISK NUMBERING

One primary feature of the SC7000/B1 Disk Controller is its ability to emulate up to eight DEC logical disk subsystems by using only four physical disk drives. This emulation is accomplished by mapping two logical disk subsystems on one physical disk drive that has double the capacity of the standard DEC subsystem. In such emulations, the logical disk drive units are mapped onto the physical disk drive units as listed in the following table:

Physical Unit Number	Logical Unit Numbers	Switch Pack
0	0 and 4	SW1
1	1 and 5	SW2
2	2 and 6	SW3
3	3 and 7	SW4

Table A-1. Disk Drives Supported by SC7000/B Disk Controller

Mfr	Model	Cylinders	Tracks	Sectors	Key	Configuration (Hex. No.)
Ampex	330	1024	16	32	330	09 through 0C
Ampex	9300	815	19	32	301	08
CDC	9715-340	711	24	32	400	16,17
CDC	9715-515	711	24	50	515A	19
CDC	9730-80	823	5	32	80	00
CDC	9730-160	823	10	32	160	03 through 05
CDC	9762	823	5	32	80	00
CDC	9766	823	19	32	300	01
CDC	9771	1024	16	64	600	18
CDC	9771	1024	16	84	825	14,15
CDC	9775	842	40	32	675	13
Century	T82RM	823	5	32	80	00
Century	T302RM	823	19	32	300	01
Fujitsu	2280	823	5	32	80	00
Fujitsu	2284	823	10	32	160	03 through 05
Fujitsu	2294	1024	16	32	330	09 through 0C
Fujitsu	2298	1024	16	64	600	18
Fujitsu	2298	1024	16	68	601	1A
Fujitsu	2312	589	7	32	84	02
Fujitsu	2351A	842	20	44/48	470	0E-11, 1B
NEC	D1510	560	30	32	331	0D
STC	8775	1124	30	32	673	12
Textor	S160	700	12	32	162	06, 07

Table A-2. Disk Drive Configurations, PROM No. 994

Configuration (Hex. No.)	Emulation	Key	Nonstandard Characteristics
00	Standard RM03	80	None
01	Standard RM05	300	None
02	Standard RM03	84	Remapped to 7 tracks, 32 sectors
03	Mapped RM80	160	Remapped to 10 tracks, 32 sectors
04	2 X RM03	160	2 standard RM03 units
05	Expanded RM02	160	823 cylinders, 10 tracks, 32 sectors RM02
06	Mapped RM80	162	Remapped to 14 tracks, 32 sectors
07	2 X RM03	162	Each remapped to 6 tracks, 32 sectors

continued on next page

Table A-2. Disk Drive Configurations, PROM 994 (continued)

Configuration (Hex. No.)	Emulation	Key	Nonstandard Characteristics
08	Expanded RM02	301	815 cylinders, 19 tracks, 32 sectors RM02
09	2 X RM80	330	Each remapped to 8 tracks, 32 sectors
0A	Mapped RM05	330	Remapped to 16 tracks, 32 sectors
0B	Expanded RM05	330	1024 cylinders, 16 tracks, 32 sectors RM05
0C	Expanded RM02	330	1024 cylinders, 16 tracks, 32 sectors RM02
0D	Mapped RM05	331	Remapped to 30 tracks, 32 sectors
0E	Expanded RM02	470	842 cylinders, 20 tracks, 44 sectors Eagle, RM02
0F	Expanded RM02	470	842 cylinders, 20 tracks, 48 sectors Eagle, RM02
10	Expanded RM80	470	842 cylinders, 20 tracks, 44 sectors Eagle, RM80
11	Expanded RM80	470	842 cylinders, 20 tracks, 48 sectors Eagle, RM80
12	2 X RM05	673	Each remapped to 15 tracks, 32 sectors RM05
13	2 X RM05	675	2 standard RM05 units
14	Expanded RM05	825	1024 cylinders, 16 tracks, 84 sectors RM05
15	Expanded RM80	825	1024 cylinders, 16 tracks, 84 sectors RM80
16	Standard RM05	400	Mapped standard RM05
17	Expanded RM05	400	Remapped to 711 cylinders, 24 tracks
18	2 X RM05	600	2 standard RM05 units
19	Expanded RM05	515A	Remapped to 711 cylinders, 24 tracks, 50 sectors
1A	Expanded RM05	601	Remapped to 1024 cylinders, 16 tracks, 68 sectors
1B	Expanded RM05	470	Remapped to 711 cylinders, 24 tracks, 48 sectors
1C	(Not Used)		
.	.		
.	.		
.	.		
37	(Not Used)		

Switch settings for each configuration are listed in Table A-3.

Table A-3. Switch Settings for Configuration Code Numbers

Conf. No.	SWn- 6	5	4	3	2	1
00	O	O	O	O	O	O
01	O	O	O	O	O	C
02	O	O	O	O	C	O
03	O	O	O	O	C	C
04	O	O	O	C	O	O
05	O	O	O	C	O	C
06	O	O	O	C	C	O
07	O	O	O	C	C	C
08	O	O	C	O	O	O
09	O	O	C	O	O	C
0A	O	O	C	O	C	O
0B	O	O	C	O	C	C
0C	O	O	C	C	O	O
0D	O	O	C	C	O	C
0E	O	O	C	C	C	O
0F	O	O	C	C	C	C
10	O	C	O	O	O	O
11	O	C	O	O	O	C
12	O	C	O	O	C	O
13	O	C	O	O	C	C
14	O	C	O	C	O	O
15	O	C	O	C	O	C
16	O	C	O	C	C	O
17	O	C	O	C	C	C
18	O	C	C	O	O	O
19	O	C	C	O	O	C
1A	O	C	C	O	C	O
1B	O	C	C	O	C	C

C = CLOSED, O = OPEN

A.2.2 SECTORING CDC DISK DRIVES AND 2351A FUJITSU DISK DRIVES

To allow CDC and Fujitsu 2351A disk drives to function properly with the SC7000/B1 Disk Controller, some alterations must be made to the sector-select switch settings described in the respective technical manuals for those disk drives.

To configure the CDC 9771 disk drive for 84 sectors/track, close switches 1 and 4 on the left six-position DIP switch and close switch 3 on the right six-position DIP switch. All other switches must be open. The two DIP switches are located on the front-most PCBA, and should be viewed from the right side of the disk drive. To configure the Fujitsu 2351A for 48 sectors/track, jumpers at location BC7 must be positioned so that bit one is jumpered 2-3 (instead of 3-4) and bit two is jumpered 6-7 (instead of 5-6), but

all other jumpers must remain positioned as specified in the Fujitsu 2351A manual.

A.2.3 DISK DRIVE CONFIGURATION SELECTION

The SC7000/B1 Disk Controller emulates three different DEC disk drive subsystems: RM03, RM05, and RM80. The RM03 subsystem has an unformatted capacity of 80 megabytes. The RM05 subsystem has an unformatted capacity of 300 megabytes. The RM80 has an unformatted capacity of 160 megabytes.

Essentially, three different disk drive configurations can be emulated:

- Each emulated DEC logical disk drive unit exists on one physical disk drive.
- Two emulated DEC logical disk drive units are mapped on one physical disk drive.
- One emulation is expanded to take advantage of a disk drive that has greater capacity.

No standard configurations require patches to the operating system or to the diagnostics. Expanded emulations are made possible by a patch as explained in the following note:

NOTE

The DEC VMS driver assumes all RM-type disk drives have 32 sectors/track. Emulex has a VMS driver patch that automatically self-sizes to each disk drive. The patched driver can handle up to 256 sectors/track. **The DEC diagnostics can not run on disk drives of nonstandard sectors/track.**

To find the configuration switch settings most suitable for a particular disk drive installation, locate disk drive model number, key and sectors in Table A-1. Note down KEY number assigned to that disk drive. If more than one model/type of disk drive are to be used in system, note down KEY number assigned to each model/type as well. Verify respective disk drive(s) to be used are hard sectored as specified in Sectors column of Table A-1.

DIP switch SW1 selects the configuration for physical disk drive unit 0. Switch SW2 selects the configuration for physical disk drive unit 1. Switch SW3 selects the configuration for physical disk drive unit 2. Switch SW4 selects the configuration for physical disk drive unit 3. Thus, the user must set the appropriate disk drive configuration hexadecimal number in each of the four DIP switches to configure the entire SC7000 Disk Controller for system operation with up to four physical disk drives. Table A-3 lists the switch settings for each configuration.

A.3 SC7000/B1 USER-SELECTABLE OPTIONS

Several other options for the SC7000/B1 Disk Controller can be user selected. The functions of the switches that select those options are listed and defined in Tables A-4, A-5, and A-6.

Table A-4. Option Switches SW5 and SW6 Settings

Option Switch	Open	Closed	Function
SW5-1	Run	Halt-Reset	Controller Run/Halt-Reset[1]
SW5-2	Disable	Enable	Dual-Access mode[3]
SW5-3			Not used[2]
SW5-4			Not used[2]
SW6-1			Not used[2]
SW6-2			Not used[2]
SW6-3			Not used[2]
SW6-4			Not used[2]

[1]Causes VAX CPU reset as well when closed if SW8-1 is also closed.
[2]Not used switches MUST BE OFF.
[3]See subsection 6.6.5.7.

Table A-5. Option Switch SW7 Settings

Option Switch	Open	Closed	Function
SW7-1			Not used[1]
SW7-2	Disable	Enable	Select physical disk drives 4--7 instead of 0--3
SW7-3			Not used[1]
SW7-4	Disable	Enable	Delay on overlapped searches to the same physical disk drive.
SW7-5	Disable	Enable	CDS Trident disk drive compatibility.
SW7-6	Disable	Enable	Dual-Port mode.
SW7-7	VAX-11/750	VAX-11/780	CPU select
SW7-8	B-Cable	A-Cable	Sector and Index signals[3]

[1]All unused switches MUST BE OFF.
[2]Must be open (OFF) for VAX-11/750 operation or closed (ON) for VAX-11/780 operation.
[3]See subsections 4.3.4 and 4.4.2.4.

Table A-6. Option Switch SW8 Settings

Option Switch	Open	Closed	Function
SW8-1	VAX-11/750	VAX-11/780	CPU reset (via AC LOW) when SW5-1 is switched ON.
SW8-2			MBA Arbitration Level[2]
SW8-3			MBA Arbitration Level[2]
SW8-4			MBA Arbitration Level[2]
SW8-5			MBA Arbitration Level[2]
SW8-6			MBA Arbitration Level[2]
SW8-7			VAX-11/750: CMI vector/address[3] VAX-11/780: Not used[4]
SW8-8	Slot 3	Slot 4	VAX-11/780: Controller Address[5] VAX-11/750: CMI vector/address[3]

[1]See subsections 4.4.2.1 and 4.5.3.1.
[2]See subsections 4.5.3.1 and 4.5.3.2.
[3]See subsection 4.4.2.2.
[4]All unused switches MUST BE OFF.
[5]See subsection 4.4.5.3.2.

A.4 BUS INTERFACE PCBA OPTION SWITCH SETTINGS

Table A-7 lists and describes functions of switches in DIP switch pack SW1 on the Bus Interface PCBA.

Table A-7. Bus Interface PCBA Option Switch SW1 Settings

Option Switch	Open	Closed	Function
SW1-1			SBI Arbitration (TR No.) Level[1]
SW1-2			SBI Arbitration (TR No.) Level[1]
SW1-3			SBI Arbitration (TR No.) Level[1]
SW1-4			SBI Arbitration (TR No.) Level[1]
SW1-5			SBI Interrupt Request Level[2]
SW1-6			SBI Interrupt Request Level[2]
SW1-7			Not used[3]
SW1-8			Not used[3]

[1]See subsection 4.5.2.1.1.
[2]See subsection 4.5.2.1.2.
[3]All unused switches MUST BE OFF.

A.5 BUS TRANSLATOR PCBA OPTION SWITCH SETTINGS

Table A-8 lists and describes functions of switches in DIP switch pack SW1 on the Bus Translator PCBA.

Table A-8. Bus Translator PCBA Option Switch SW1 Settings

Option Switch	Open	Closed	Function
SW1-1	Disable	Enable	Early TR arbitration for SC7000 Disk Controller in slot 3 of V-MASTER.[1]
SW1-2	Disable	Enable	Early TR arbitration for SC7000 Disk Controller in slot 4 of V-MASTER.[1]
SW1-3	Enable		Continuous Clock generation in both controllers in V-MASTER and FAULT LED on each controller remains unlit during bootstrap operation or during run of microdiagnostic test programs.[2]
		Disable	No continuous Clock generation in both controllers in V-MASTER and FAULT LED on each controller blinks during bootstrap operation or during run of microdiagnostic test programs.[2]
SW1-4			Not used.[3]

[1] See subsection 4.5.2.2.1.
[2] See subsection 4.5.2.2.2.
[3] Not used switches MUST BE OFF.

B.1 OVERVIEW

This appendix provides modification instructions for moving the Sector and Index signals from the A-Cable to the B-Cable for commonly used disk drives. This appendix is divided into eight subsections, as listed in the following table:

Subsection	Title
B.1	Overview
B.2	CDC 9762
B.3	CDC 9730
B.4	CDC 9766
B.5	CDC 9448
B.6	Trident Disk Drives
B.7	Fujitsu Disk Drives
B.8	Ampex Capricorn

B.2 CDC 9762

Remove (Ch. I)	Add (Ch. I)
B01-06B to JA82-18B	B01-06B to JA82-43B
B01-06A to JA82-18A	B01-06A to JA82-44A
B01-05B to JA82-25B	B01-05B to JA82-45B
B01-05A to JA82-25A	B01-05A to JA82-45A

Remove (Ch. II)	Add (Ch. II)
B03-06B to JA83-18B	B03-06B to JA83-43B
B03-06A to JA83-18A	B03-06A to JA83-44A
B03-05B to JA83-25B	B03-05B to JA83-45B
B03-05A to JA83-25A	B03-05A to JA83-45A

Rework Transmitter PCBA FTVV in location B01 (Ch. I) and B03 (Ch. II). Locate jumper at center bottom of PCBA (as viewed with connector toward right side). Remove jumper and reinsert one set of holes lower; i.e., from center hole to hole below original jumper. Remove letter "F" from PCBA type designation FTVV and mark a "G" in its place so that PCBA type becomes GTVV.

NOTE

On later models of the 9762 CDC ships units with an enhancement feature which allows easy switch-over to the B-Cable. User need only remove the jumper plug from **B07** of the logic chassis backpanel.

B.3 CDC 9730

Rework Transmitter-Receiver PCBA CFAX in location A04 (Ch. I) and B04 (Ch. II). When viewing PCBA with connector toward right side, locate four jumpers to left of I/O connectors and above terminator ground lug. Bottom end of jumpers must be removed from holes to which they are soldered and moved to holes immediately above. Next, find small jumper to right of third IC from connector edge of PCBA on bottom row of ICs. This jumper must be removed and reinserted so it connects top and middle holes instead of the original connection of bottom and middle holes. This connection ungates the driver for the Sector and Index signals.

Remove letter "C" from PCBA type designation CFAX and mark a "D" in its place so PCBA type becomes DFAX.

B.4 CDC 9766

Remove (Ch. I)		Remove (Ch. II)	
Sector +	J4-55	Sector +	J4-55
Sector -	J4-25	Sector -	J4-25
Index +	J4-48	Index +	J4-48
Index -	J4-18	Index -	J4-18

Move Wire (Ch. I)	Origin	From	To
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Ch II)	Origin	From	To
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

Rework Transmitter PCBA FTVV in location A01 (Ch. I) and A03 (Ch. II). Locate jumper at center bottom of PCBA; viewed with connector toward right side. Remove jumper and reinsert one set of holes lower; i.e., from center hole to hole below original jumper. Remove letter "F" from PCBA type designation FTVV and mark "G" in its place so PCBA type becomes GTVV.

NOTE

On later models of the 9766 CDC ships units with an enhancement feature which allows easy switch-over to B-Cable: Cut cable tie that holds PD90 to I/O cable and plug PD() into JD90 pins 13 and 14 (Ch. I) and pins 11 and 12 (Ch. II) as indicated on top of connector.

B.5 CDC 9448

Sector and Index signals are on both the A-Cable and B-Cable. No modification required.

B.6 TRIDENT DISK DRIVES

Sector and Index signals are on both the A-Cable and B-Cable. No modification required.

B.7 FUJITSU DISK DRIVES

Sector and Index signals are on both the A-Cable and B-Cable. No modification required.

B.8 AMPEX CAPRICORN

To place Sector and Index signals on both the A-Cable and B-Cable, connect the following jumpers on the I/O PCBA:

E1 to E2
E3 to E4
E5 to E6
E7 to E8.

BLANK

Appendix C
OPERATION OF DIAGNOSTICS

C.1 OVERVIEW

This appendix contains step-by-step procedures for running the DEC RH750, RH780, and RM03/RM05/RM80 diagnostics. Emulex recommends running the diagnostic programs in the order presented (skip the programs not intended for your disk drive). Additional information about the Diagnostic Supervisor and about running the diagnostic programs can be found in the "VAX Diagnostic System User's Guide" (DEC Publication No. EK-VX11D-UG-001) or by typing HELP when in the Diagnostic Supervisor.

NOTE

Only disk drives of standard capacity (size) can be run with DEC diagnostics. For disk drives of nonstandard size, Emulex's Formatter and Reliability tests must be used.

The RM03/RM05 DEC Formatter Diagnostic, EVRAC, must be revision 5.2 or later. Older versions of this diagnostic have a bug which does not allow the bad block file to be written as required when using non-DEC media. The EVRAC revision level may be checked by running the diagnostic as described in subsection C.6. After EVRAC has been loaded, the diagnostic identifies itself and its revision.

This appendix is divided into 10 subsections, as listed in the following table:

Subsection	Title
C.1	Overview
C.2	Loading and Starting
C.3	ECCAA - RH750 Diagnostic
C.4	ESCAA - RH780 Diagnostic
C.5	EVRDA - RM03/RM05/RM80 Diskless Diagnostic
C.6	EVRAC - VAX RM03/RM05 Disk Formatter
C.7	EVRDB - VAX RM03/RM05 Functional Diagnostic
C.8	EVRGA - RM80 Formatter
C.9	EVRGB - RM80 Functional Diagnostic
C.10	EVRAA - RM Disk Reliability Test

C.2 LOADING AND STARTING

Loading and starting procedures for the VAX-11/750 and VAX-11/780 CPU systems differ slightly.

C.2.1 VAX-11/750 CPU SYSTEM

To allow the Diagnostic Supervisor to be bootstrapped on a command from the system console, the console must be in the Console I/O mode, as indicated by a >>> prompt symbol. If that >>> prompt symbol is not present, type CTRL P. Typing CTRL P places the console in the Console I/O mode. To bootstrap the Diagnostic Supervisor, turn the BOOT DEVICE switch on the CPU panel to the proper position for the bootstrap device to be used, then type B or B/10 to specify the system disk. Once the Diagnostic Supervisor has been loaded, it issues a DS> prompt symbol.

If the Diagnostic Supervisor was bootstrapped from a cassette, remove that cassette from the disk drive and replace it with the cassette that contains the RH750 Diagnostics.

The Massbus Adapters (RH0, RH1, RH2 or RH3) and the disk drives to be tested (DRBn) must be ATTACHed to inform the Diagnostic Supervisor of their presence and of their type.

1. ATTACH the RH750 (SC7000): specify its device type (**RH750**), its link to the CPU (**CMI**), its generic device name and address (RH0, **RH1**. RH2 or RH3) and its BR level (**5**):

```
DS>  ATTACH  RH750  CMI  RH1  5
```

2. ATTACH the disk drive: specify the type (**RM03**. RM05 or RM80), link to the CPU (RH0, **RH1**, RH2 or RH3) and generic device name (**DRB0**, DRB1, DRB2 or DRB3):

```
DS>  ATTACH  RM03  RH1  DRB0
```

A Massbus Adapter (MBA) must be ATTACHed to ATTACH a disk drive that is to be connected to the MBA, even if no diagnostic routines are intended to be run on the MBA. One ATTACH statement is required for each MBA device. Substitute the appropriate variable for each new ATTACH statement.

After ATTACHing the group of MBA devices to be tested, SELECT the specific MBA devices that are to be tested.

3. SELECT the MBA to be tested: use its generic device name:

```
DS>  SELECT  RH1
```

4. SELECT the disk drive to be tested: use its generic device name:

```
DS>  SELECT  DRB0
```

All MBA devices to be tested must be SELECTed by using individual SELECT statements. When more than one MBA device of the same type has been SELECTed, tests run against that type of device are run sequentially; lowest numbered device first.

To allow the operator to monitor testing progress, the trace option can be SET. For diskless and functional diagnostics, this trace option greatly increases test time.

5. SET the trace option by typing the following statement:

```
DS>  SET  TRACE
```

The next step is to LOAD the diagnostics. The default load device is that device from which the Diagnostic Supervisor was bootstrapped.

6. LOAD a diagnostic program (in this instance, **ECCAA**) by typing the following statement:

```
DS>  LOAD  ECCAA
```

Only one diagnostic program may be LOADed at a time.

Once LOADed, the program may be STARTed (or reSTARTed) in any section or test any number of times (without redoing any of the operations thus far described).

7. START the test that is currently in memory by typing the following statement:

```
DS>  START
```

   All tests and/or sections of tests are then run one time.

8. START the diagnostic: specify the TEST number(s) to be run by typing the following statement:

```
DS>  START/TEST:first:last
```

   Substitute the decimal number of the first test to be run for the word **first** and the number for the last test to run for the word **last.** All the tests between those two numbers are then run. To run only one test, the **first** and **last** numbers are the same.

9. START the diagnostic: specify the TEST numbers and the number of PASSes of all tests selected by typing the following statement:

```
DS>  START/TEST:first:last/PASS:n
```

Substitute a decimal number for the letter n.

10. START the diagnostic: specify a SECTION name by typing the following statement:

```
DS>  START/SECTION:name
```

Substitute the name of a SECTION of the diagnostic for the word **name**.

The diagnostic program can be returned to the Diagnostic Supervisor by typing CTRL C. The program may then be aborted by typing ABORT or the program can be resumed (after possible flag changing) by typing CONT.

C.2.2 VAX-11/780 CPU SYSTEM

To allow the Diagnostic Supervisor to be bootstrapped on a command from the system console, the console must be in the Console I/O mode, as indicated by a >>> prompt symbol. If that >>> prompt symbol is not present, type CTRL P. Typing CTRL P places the console in the I/O mode.

To load the Diagnostic Supervisor from a floppy disk, load the DS diskette into the floppy disk drive and type "B" at the console. If the DS is on the system disk, typing "B SB0" causes the Diagnostic Supervisor to be loaded.

Once the diagnostic supervisor has been loaded, it issues a DS> prompt symbol.

If the Diagnostic Supervisor was bootstrapped from a floppy disk, remove that floppy disk from the disk drive and replace it with the floppy disk that contains the RH780 diagnostics.

The MBAs (RHn) and disk drives to be tested (DRBn) must be ATTACHed to inform the Diagnostic Supervisor of their presence and of their type.

1. ATTACH the RH780 (SC7000): specify its device type (**RH780**), its link to the CPU (**SBI**), its generic device name and address (RH0, **RH1**, RH2 or RH3), TR level (8, 9, **10** or 11), and BR level (**5**):

```
DS>  ATTACH  RH780  SBI  RH1  10  5
```

2. ATTACH the disk drive: specify the type (**RM03**), RM05 or RM80), link to the CPU (RH0, **RH1**, RH2 or RH3) and generic device name (**DRB0**, DRB1, DRB2 or DRB3):

```
DS>  ATTACH  RM03  RH1  DRB0
```

An MBA must be ATTACHed to ATTACH a disk drive that is to be connected to it, even if no diagnostics are intended to be run on the MBA. One ATTACH statement is required for each MBA device. Substitute the appropriate variable for each new statement. After ATTACHing the group of MBA devices to be tested, SELECT the specific MBA devices that are to be tested.

3. SELECT the MBA to be tested: use its generic device name:

```
DS>  SELECT  RH1
```

4. SELECT the disk drive to be tested: use its generic device name:

```
DS>  SELECT  DRB0
```

All MBA devices that are to be tested must be SELECTed by using individual SELECT statements. When more than one MBA device of the same type has been SELECTed, tests run against that type of device are run sequentially; lowest numbered device first.

To allow the monitor to monitor testing progress, the trace option should be SET.

5. SET the trace option by typing the following statement:

```
DS>  SET TRACE
```

The next step is to LOAD the diagnostics. The default load device is that device from which the Diagnostic Supervisor was bootstrapped.

6. LOAD a diagnostic program (in this instance **ESCAA**) by typing the following statement:

```
DS>  LOAD ESCAA
```

Only one diagnostic program may be LOADed at a time.

Once LOADed, the diagnostic program may be STARTed (or reSTARTed) in any section or test any number of times (without redoing any of the operations thus far described.

7. START the test that is currently in memory by typing the following statement:

```
DS>  START
```

   All tests and/or sections are run one time.

8. START the diagnostic: specify the TEST number(s) to be run by typing the following statement:

```
DS>  START/TEST:first:last
```

Substitute the decimal number of the first test to be run for the word **first** and the number of the last test to be run for the word **last**. All the tests between those two numbers are then run. To run only one test, the **first** and **last** numbers are the same.

9. START the diagnostic: specify the TEST numbers and the number of all PASSes of all tests selected by typing the following statement:

```
DS>  START/TEST:first:last/PASS:n
```

Substitute a decimal number for the letter **n**.

10. START the diagnostic: specify a SECTION name by typing the following statement:

```
DS>  START/SECTION:name
```

Substitute the name of a SECTION of the diagnostic for the word **name**.

The diagnostic program can be returned to the Diagnostic Supervisor by typing CTRL C. the diagnostic program may then be aborted by typing ABORT, or the diagnostic program can be resumed (after possible flag changing) by typing CONT.

C.3 ECCAA - RH750 DIAGNOSTIC

To run this diagnostic program, SELECT the appropriate RH750 (RH0, RH1, RH2 or RH3). It is not necessary to ATTACH or SELECT a disk drive.

This diagnostic provides functional verification and testing of the RH750 MBA portion of the SC7000 Disk Controller. Much of the diagnostic uses the Diagnostic Register which simulates signals from the Massbus. Since the SC7000 Disk Controller does not have an actual Massbus, it is not possible to run those tests which make use of the Massbus simulation function. Tests 1, 2, 3, 5, 6 and 11 run without errors and test the MBA Controller registers and Map registers. Test 11 requires disk drive zero to be on line.

C.4 ESCAA - RH780 DIAGNOSTIC

To run this diagnostic, SELECT the appropriate RH780 (RH0, RH1, RH2 or RH3). It is not necessary to ATTACH or SELECT a disk drive.

This diagnostic provides functional verification and testing of the RH780 MBA portion of the SC7000 Disk Controller. Much of the diagnostic uses the Diagnostic Register which simulates signals from the Massbus. Since the SC7000 Disk Controller does not have an actual Massbus, it is not possible to run those tests which use the Massbus simulation function. Tests 1, 2, 3, 5, and 6 run without errors and test the MBA Controller registers and Map registers.

C.5 EVRDA - RM03/RM05/RM80 DISKLESS DIAGNOSTIC

This diagnostic is a stand-alone program which uses functional and diagnostic means to verify the operational capability of the SC7000 Disk Controller independently of the disk drive(s).

Part of this diagnostic operates the disk drive in the Diagnostic mode. The Diagnostic mode is not fully implemented in the SC7000 Disk Controller; therefore, with the disk drive cycled down, only Tests 1 through 23 are run without errors. The functions performed by this diagnostic are very limited and do not involve any Data Transfer operations.

C.6 EVRAC - VAX (RM03/RM05) DISK FORMATTER

The disk formatter diagnostic program consists of six sections, each made up of one or more common parts or tests. When the formatter diagnostic program is started, the Initialization code requests a channel be assigned for the selected disk, builds a device-dependent table, and then reads the contents of the homeblock. If the disk pack is labeled SCRATCH, the program proceeds. If the program is unable to read the contents of the homeblock or if the disk pack is not labeled SCRATCH, the user is asked whether the program is or is not to proceed.

Initialization adjusts QIO buffer sizes. QIO buffer size (capacity) depends on the mode in which the programming is being run. If the program is being run in the User mode under VMS operation, the QIO buffer size is set to 35 pages. This size allows one-track Data Transfer operations for the largest disk. If the program is being run in the Stand-Alone mode, the QIO buffer size is set to 110 pages. This size allows multiple-track Data Transfer operations.

C.6.1 PACKINIT SECTION

This section formats and writes a bad sector file with all zero entries on all sectors of the last track. The section then reads the contents of the bad sector file and verifies the file conforms to the proper format and that all physical disk addresses are within the limits of the disk drive. (If contents of the bad sector file cannot be read or if the bad sector file is corrupt, the program is aborted.)

After successfully reading the contents of the bad sector file, the disk pack is formatted one track at a time. At completion of the format process, a Write/Read sequence is performed on every sector of the disk pack. This operation constitutes a surface analysis. During this surface analysis, any bad sector discovered is flagged and added to the contents of the bad sector file. The homeblock is written with the name SCRATCH in a format which allows the disk diagnostics to detect a valid label name, but which makes the homeblock appear invalid to the VMS.

This section should never be run unless the user has verified the disk subsystem is functioning correctly and that the bad sector file is indeed missing or corrupt. This section must be used on all foreign disk packs and on those disk packs that have not had bad sector files previously written on the pack. The user should be aware that an updated bad sector file is not written on the disk pack until the end of the Verify operation.

C.6.2 FORMAT SECTION

This section reads and validates the contents of the bad sector file. If the contents of the bad sector file cannot be read, or if the bad sector file is corrupt, the disk formatter diagnostic program is aborted. After successfully reading the contents of the bad sector file, the disk pack is formatted one track at a time. At the completion of the format process, a surface analysis is performed, and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

C.6.3 VERIFY SECTION

This section reads and validates the contents of the bad sector file. If the contents of the bad sector file cannot be read, or if the bad sector file is corrupt, the disk formatter diagnostic program is aborted. After successfully reading the contents of the bad sector file, a surface analysis of the disk pack is performed, and any bad sector discovered is flagged and added to the bad sector file. The homeblock is written with the name SCRATCH.

The user should be aware that the updated bad sector file is not written on the disk pack until the end of this VERIFY section.

C.6.4 READALL SECTION

This section reads the contents of every sector on a disk pack and any data errors found are printed in a Head Map Error report. On a disk drive known to be good (without formatting errors), this section can be used to search for data errors on a disk pack. Conversely, by using a known good disk pack, or one with known errors, this section can be used to check the Read capability of the disk drive.

C.6.5 FLAGBAD SECTION

This section allows the user to manually update the bad sector file by prompting the user for the address of the bad block. After the user has selected all the bad blocks to be flagged, the disk formatter diagnostic program rewrites the bad block file and clears the Bad Sector flag in the header word of each bad block. The disk formatter diagnostic program then destroys the file directory by rewriting the homeblock. This rewrite is done to ensure no files contain holes. The disk formatter diagnostic program then reads the contents of the bad block file and displays those contents at the console.

This section should not be used unless the user is familiar with the structure of the bad sector file and understands the significance of updating that file. Any data on the disk is not preserved. The home block is rewritten with the name SCRATCH.

C.6.6 HELP SECTION

This section provides default information. Section names and functions are identified.

Program and Event Flags

Quick - The Quick flag reduces the number of data patterns used in the VERIFY section from three to one.

Event Flag 23 - This flag causes the starting disk address to be printed for each step in a section.

Event Flag 22 - This flag causes the starting disk address to be printed once every 100 cylinders.

Event Flag 21 - This flag causes error messages to be printed in brief format.

Event Flag 20 - This flag causes single-track Data Transfer operations in the Surface Analysis Test (Stand-Alone mode only).

Format and Verify Time

Disk Drive	Normal Time	Quick Time
RM03	14 minutes	7 minutes
RM05	60 minutes	37 minutes

C.7 EVRDB - VAX RM03/RM05 FUNCTIONAL DIAGNOSTICS

This diagnostic program contains a set of 40 tests which verify the integrity of the SC7000 Disk Controller and disk drives under test. The set of tests include: Data Transfer tests, Seek tests, Timing tests, and Manual Intervention tests. Tests 34 through 37 are Manual Intervention tests which are invoked by running the section labeled MANUAL.

This functional diagnostic program requires mounting a scratch disk pack and placing that pack in the On-Line mode.

C.8 EVRGA - RM80 FORMATTER

The function of this diagnostic program is to format the RM80 HDA. EVRGA is a section-selectable formatter diagnostic program with seven sections, instead of a test-selectable formatter diagnostic program. Section selection prevents accidental destruction of data. When the formatter is started, the Initialization code requests a channel be assigned for the selected disk, builds a device-dependent table, and then reads the contents of the homeblock. If the disk pack is labeled SCRATCH, the formatter diagnostic program proceeds. If this program is unable to read the contents of the homeblock or if the disk pack is not labeled SCRATCH, the contents limit of the buffer is set to 35 pages. This limit allows one-track Data Transfer operations of the largest disk. If this program is to be run in the Stand-Alone mode, the buffer capacity is set to 110 pages. This buffer capacity allows multiple-track Data Transfer operations (up to three tracks on an RM80). If this program is to be run in the User mode, the buffer capacity is set to 35 pages.

C.8.1 HDAINIT SECTION

This section first asks the user which files are to be initialized; the Skip Sector file or the Bad Sector file. When the file to be initialized is determined, that track on which the file resides is formatted and a Skip Sector file or Bad Sector file, with all zeros entered, is written and verified.

This section should never be run unless the user has verified the disk subsystem is functioning correctly and the Bad Sector file or Skip Sector file is indeed missing or is corrupt. This section must be used on all foreign HDAs and on those HDAs that have not had a Bad Sector file previously written on the HDA. The Bad Sector File and the Skip Sector file must have the same serial number.

C.8.2 FORMAT SECTION

This section reads and validates the contents of both the Bad Sector files and the Skip Sector files. (If the contents of these files cannot be read or if they are corrupt, this formatter diagnostic program is aborted.) After the contents of both the Bad Sector file and Skip Sector file have been read successfully, the

HDA is formatted one track at a time. When the formatting process is completed, a surface analysis is performed and any bad sector discovered is flagged and added to the Bad Sector File or the Skip Sector file. The file in which any bad sector(s) is deposited depends on the error type and the error position. The homeblock is written with the name SCRATCH.

C.8.3 VERIFY SECTION

This section reads and validates the contents of both the Bad Sector files and the Skip Sector files. (If the contents of these files cannot be read or if they are corrupt, this formatter diagnostic program is aborted.) After the contents of both the Bad Sector file and Skip Sector file have been read successfully, the disk pack surface is analyzed and any bad sector discovered is flagged and added to the Bad Sector file or the Skip Sector file. The file in which any bad sector(s) is deposited depends on the error type and the error position. The homeblock is written with the name SCRATCH.

The user should be aware that the updated Bad Sector file is not written on the disk pack until the end of this VERIFY section.

C.8.4 READALL SECTION

This section reads the contents of every sector on the HDA and any data errors found are printed in a Head Map Error report. On a disk drive known to be good (no formatting errors), this section can be used to search for data errors on a HDA. Conversely, by using an HDA that is known to be good or by using an HDA with known errors, this section can be used to check the Read capability of the disk drive and the SC7000 Disk Controller.

C.8.5 UPDATE SECTION

This section allows the user to manually update the Bad Sector file or Skip Sector file. It prompts the user for the address of each bad sector. After the user has selected all the bad sectors to be flagged, this formatter diagnostic program rewrites the Bad Sector file or the Skip Sector file. This section should not be used unless the user is familiar with the skip sectoring algorithm incorporated by the RM80. The user must also understand the structure of the Bad Sector File and the significance of updating that file. Any data on the disk is not preserved.

C.8.6 REBUILD SECTION

This section allows the user to rebuild a Bad Sector file or a Skip Sector file if such a file should become destroyed. The track where the selected file is located is formatted first, then a file is written in which all entries are zeros. After this file is written, the rest of the procedure in this section is performed in the same way as is the procedure of the UPDATE section.

C.8.7 HELP SECTION

This section provides default information. Section names and functions are identified.

Program and Event Flags

Quick - The Quick flag reduces the number of tracks read from five to one.

Event Flag 23 - This flag causes the starting disk address for each step in a section to be printed.

Event Flag 22 - This flag causes the starting address to be printed once every 100 cylinders.

Event Flag 21 - This flag causes error messages to be printed in brief format.

Event Flag 20 - This flag causes single-track Data Transfer operations in the Surface Analysis Test (Stand-Alone mode only).

Event Flag 19 - This flag causes only the FE cylinders to be formatted.

Event Flag 18 - This flag causes the FORMAT section to bypass verification.

Format and Verify Time

Disk Drive	Normal Time	Quick Time
RM80	33 minutes	16 minutes

C.9 EVRGB - RM80 FUNCTIONAL DIAGNOSTIC

This diagnostic program contains a set of 40 tests which verify the integrity of the SC7000 Disk Controller and the disk drives being tested. The set of tests include: Data Transfer tests, Seek tests, Timing tests, and Manual Intervention tests. The tests require the disk drive to be on line. Test 40 is a Manual Intervention test which is invoked by running the section named MANUAL.

C.10 EVRAA - RM DISK RELIABILITY TEST

This diagnostic program requires a formatted disk pack (or HDA) to be on each disk drive under test. The disk packs should not be "mounted". Each disk pack must have a volume name of SCRATCH or DIAGNOSTIC. If neither name is recorded on the home block of the disk pack, this diagnostic program aborts any further activities on all disk drives. If the disk pack is not formatted, or if it is desired to run this diagnostic program while using a disk pack with some other volume name, then the appropriate formatter program must

be run first. The formatter program gives the volume the name of SCRATCH after the Format operation is completed. This diagnostic program has six sections. Only one section is to be run for each START statement.

C.10.1 QUALIFICATION SECTION

This section issues each of the disk drive function commands to ensure the disk drive(s) under test can support all those commands. After all functions that do not involve Data Transfer operations have been tested, this test issues a Write, Write Check and Read command sequence to a group of disk addresses. The goal of the Read/Write portion of this test is to access a sector on every cylinder of every track (head) without destroying the home block or the Bad Sector file located on the last track of the last cylinder. The test must be completed in less than one minute.

C.10.2 SEEK TIMING SECTION

This section performs Seek operations between cylinder 000 and the following cylinders: 001, 002, 004, 008, 016, 032, 064, 128, 256, and the last cylinder. Each Seek operation range is timed and an average time is calculated. The results are presented on the console.

C.10.3 MEDIA TEST SECTION

This section Writes and Write Checks every sector on the disk by using an entire track for each operation. Any sector in error is not reported it it is already in the Bad Sector file located on the last track of the last cylinder. Five patterns are written onto each sector over the entire disk pack. Each pattern consists of a quadword which is replicated 64 times in each sector. The Media Test uses the following five patterns:

```
1.   F00FF00FF00FF00F     ;worst case for RH780 or RH750
2.   EC6DEC6DEC6DEC6D     ;worst case for media
3.   A5A5A5A5A5A5A5A5     ;alternating ones and zeros
4.   123456789ABCDEF0
5.   FEDCBA9876543210
```

After all sectors have been written by using the above patterns, the test enters a Random mode where random patterns are written to randomly selected disk addresses.

C.10.4 MULTI-DRIVE TEST SECTION

This section tests up to eight disk drives by transferring random data to randomly selected disk addresses for all selected disk drives at the same time. That is, all transfers are issued in parallel for those disk drives attached to the SC7000 Disk Controller. The functions are performed in the following sequence:

1. Drive Clear command
2. Write random data
3. Write Check data
4. Read data
5. Data compare

C.10.4.1 Nocustomer Test

This test is the same as the Multi-Drive Test, except on an RM80 fixed-media disk drive, the entire physical area of the media -- not just the FE cylinders -- is used.

C.10.4.2 Conversation Mode

The Conversation Mode subsection is a set of diagnostic routines that allow the user to design and run simple tests with minimum difficulty. The program prompts the user on the information needed to customize the test. Data Pattern code three selects random data. Functions may be a sequence of READ, WRITE, etc. and must end with END.

Running default disk addresses can eventually destroy the homeblock and the Bad Sector file. Detected errors which are already flagged in the Bad Sector file are not inhibited as in the Multi-Drive Test.

Appendix D
VAX NUMBERS QUICK REFERENCE

D.1 OVERVIEW

This appendix contains three tables that provide quick reference for Base Addresses, and byte offsets for Internal and External registers.

VAX-11/780 Base Address

20008000 - TR4
2000A000 - TR5
2000C000 - TR6
2000E000 - TR7
20010000 - TR8
20012000 - TR9
20014000 - TR10
10016000 - TR11

VAX-11/750 Base Address

F28000 MBA 0
F2A000 MBA 1
F2C000 MBA 2

Internal Register Byte Offsets (Hex)

00 - MBA Configuration/Status Register (MBACSR) (VAX-11/780 only)
04 - MBA Control Register (MBACR)
08 - MBA Status Register (MBASR)
0C - MBA Virtual Address Register (MBAVAR)
10 - MBA Byte Count Register (MBABCR)
14 - MBA Diagnostic Register (MBADR)
18 - MBA Selected Map Register (MBASMR) (VAX-11/780 only)
1C - MBA Command Address Register (MBACAR)

800 to BFC - MBA Map Registers

External (Disk Drive) Register Byte Offsets (Hex)

Register		0	1	2	3	4	5	6	7
Control/Status 1	(RMCS1)	400	480	500	580	600	680	700	780
Drive Status	(RMDS)	404	484	504	584	604	684	704	784
Error 1	(RMER1)	408	488	508	588	608	688	708	788
Maintenance 1	(RMMR1)	40C	48C	50C	58C	60C	68C	70C	78C
Attention Summary	(RMAS)	410	490	510	590	610	690	710	790
Disk Address	(RMDA)	414	494	514	594	614	694	714	794
Drive Type	(RMDT)	418	498	518	598	618	698	718	798
Look Ahead	(RMLA)	41C	49C	51C	59C	61C	69C	71C	79C
Serial Number	(RMSN)	420	4A0	520	5A0	620	6A0	720	7A0
Offset	(RMOF)	424	4A4	524	5A4	624	6A4	724	7A4
Desired Cylinder	(RMDC)	428	4A8	528	5A8	628	6A8	728	7A8
Holding	(RMHR)	42C	4AC	52C	5AC	62C	6AC	72C	7AC
Maintenance 2	(RMMR2)	430	4B0	530	5B0	630	6B0	730	7B0
Error 2	(RMER2)	434	4B4	534	5B4	634	6B4	734	7B4
ECC Position	(RMEC1)	438	4B8	538	5B8	638	6B8	738	7B8
ECC Pattern	(RMEC2)	43C	4BC	53C	5BC	63C	6BC	73C	7BC

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